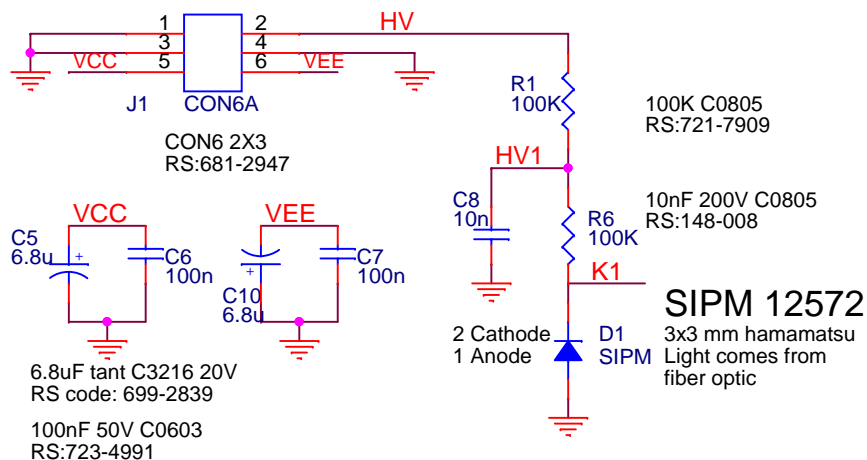


it carries the supplies: VCC (5V), VEE (-5V), GND and HV (70V) from external (different from ampli\_MPPC)

## NETWORK



The diagram shows a two-stage preamplifier. The first stage is a BJT common-emitter amplifier using a BFR182 NPN transistor (Q1). The input signal  $V_{in1}$  is coupled through capacitor  $C_{12}$  (10nF) to the base of Q1. The base is biased by a voltage divider consisting of resistors  $R_2$  (3.9K) and  $R_9$  (4.7K) connected to  $V_{CC}$  and  $V_{EE}$  respectively. A bypass capacitor  $C_3$  (2.2pF) is connected from the base to  $V_{CC}$ . The emitter of Q1 is connected to  $V_{EE}$  through resistor  $R_7$  (6.8K) and is bypassed to ground by capacitor  $C_{15}$  (100nF). The collector of Q1 is connected to  $V_{CC}$  through resistor  $R_3$  (82) and is bypassed to  $V_{CC}$  by capacitor  $C_1$  (100nF). The output of the first stage,  $V_{13}$ , is coupled through capacitor  $C_9$  (100nF) to the non-inverting input (IN+) of the second stage. The second stage is an op-amp buffer using an OPA694 op-amp (U1). The non-inverting input (IN+) is also connected to  $V_{CC}$  through resistor  $R_5$  (82). The inverting input (IN-) is connected to the output (OUT) through resistor  $R_1$  (51) and to  $V_{EE}$  through resistor  $R_2$  (270). The op-amp is powered by  $V_{CC}$  and  $V_{EE}$  with decoupling capacitors  $C_4$  (100nF) and  $C_{14}$  (100nF) respectively. The final output of the preamplifier is  $V_{17}$ , which is coupled through capacitor  $C_{11}$  (100nF) to the next stage.

All components are in package 0603.  
Only C=10n, is in package C0805.

[illegible]

NO annotate;  
NO C2, C13,

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