Torus Interlock Checklist for KPP

Date: January 19, 2017
Time: 8:30 – 9:00

Attendees: Pablo Campero, Probir Ghoshal, Tyler Lemon, Nick Sandoval

1. Updated Torus timeline for KPP.
    - 1.1. Started cool down to 4.5 [K] at 8:30AM 2017-01-19.
    - 1.2. Pablo Campero and Tyler Lemon can start interlock checklist on Monday 2017-01-23.
    - 1.3. Deadline for implementing digital filters in Fast-Daq 2017-01-23.
    - 1.4. Interlock checklist deadline Tuesday 2017-01-24.

2. Interlock checklist for KPP
    - 2.1. Will not do all checks in checklist.
        - 2.1.1. Only 18 of 50 needed because full-current commissioning requires more rigorous checklist.
    - 2.2. Deadline for finishing checklist 2017-01-24.

3. Fast-Daq digital filter.
    - 3.1. Filtering put into FPGA VI rather than in Real-Time VI.
    - 3.2. Filtering will be critical for Solenoid, as interlock thresholds will be lower.
        - 3.2.1. If digital filters unable to lower amplitude of noise to an acceptable level, hardware solution will be required.
    - 3.3. If needed, Torus can run without filtering for KPP.
        - 3.3.1. Torus is still set up as it was for full-current commissioning with comparators causing false trips taken out of interlocks.

4. Digital filter testing
    - 4.1. Tyler Lemon will continue to test digital filters.
    - 4.2. Will test two types of filters:
        - 4.2.1. Notch filters centered at 60 [Hz] with bandwidths ranging from ±10 [Hz] to ±30 [Hz].
        - 4.2.2. Lowpass filter with cutoff frequency at 50 [Hz].
    - 4.3. Do not have to wait for approval to start testing.
        - 4.3.1. Tyler will still send email notification that testing will start.