

THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY

12000 Jefferson Avenue Newport News, VA 23606 HALL B PROCEDURE NO.: B00000401 –P027 Rev -

TITLE: Hall B Pre-Power-Up Interlock Checkout Procedure

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DATE: 10 / 03 / 2016

Intended Checker and Approvers:

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3. APP: 3rd Approver (if necessary)

REV.	ECO#	DESCRIPTION	BY	СНК.	APP.	APP.	DATE
		SUMMARY OF CHANGES	FROM PR	EVIOUS I	REVISIO	N:	

Goals – Ensure Torus magnet interlock systems are operational prior to powered-up operation (some need to be checked prior to low-current operation, all need to be complete prior to full-current operation)

 Perform all interlock checks. Some require the magnet to be full of liquid helium and nitrogen

Administrative Requirements

During and after cooldown, complete the appropriate items in Pre Power Up interlock Checklist below. Upload a copy of the completed checklist to the Torus ELOG https://logbooks.jlab.org/book/hbtorus

	Checks t	a be performed prior to injecting current to magnet (law current as a section)
		to be performed prior to injecting current to magnet (low-current operation) The dware Interlock
1101/2 17		ille and the state of the state
1/24/2017	TL/PC	Test Hardwire interlock PLC Chassis watchdog
		Reset the MPS, Reference DWG B00000-09-00-0153
	V	Remove Timer Relay TYCO CNT-35-96 from DIN socket, wait 5 seconds
		Verify that the fast dump breaker has opened
	/	Verify that the SOE indicates "PLC Chassis Watchdog" via EPIcs, had to
	~	Reinstall Timer Relay TYCO CNT-35-96 into DIN socket, wait 30 seconds
	/	Clear the interlock fault on the GUI or "PLC Expert Screen"
1/14/2017	TL/PC	Test Hardwire Interlock Current lead water flow (1.4GPM switch)
		Reset the MPS. Reference DWG B00000-09-00-0160 Rev A
		Verify the current lead flow switch circuit is closed
		Verify that water is flowing through the current leads
	~	Temporarily jumper across the 1.2 GPM switch, Wire 160330
	~	Slowly close the current lead water supply valve
	/	Verify that the fast dump breaker has opened takes several minutes to trit
	~	Verify that the SOE indicate "Current Lead Water Flow"
		Unjumper the wire across the 1.2 GPM switch
	~	Slowly open the current lead water supply valve
	/	Clear the interlock fault on the GUI or "PLC Expert Screen"
1/24/2017	TL /PC	Test Hardwire Interlock Current lead water flow (1.2GPM switch)
.[[~	Reset the MPS. Reference DWG B00000-09-00-0160 Rev A
		Verify the current lead flow switch circuit is closed
	/	Verify that water is flowing through the current leads — \$ 1 Note: not an immediate trip, Temporarily jumper across the 1.4 GPM switch, Wire 160330 takes sound minutes to trip
		Temporarily jumper across the 1.4 GPM switch, Wire 160330 takes source) minutes to trip
	V	Slowly close the current lead water supply valve
	/	Verify that the fast dump breaker has opened
	/	Verify that the SOE indicate "Current Lead Water Flow"
	/	Unjumper the wire across the 1.4 GPM switch
	V	Slowly open the current lead water supply valve
	V	Clear the interlock fault on the GUI or "PLC Expert Screen"
1/24/2017	TL/pc	Test Hardwire Interlock VT Cable Interlock
7	-	Reset the MPS. Reference DWG B00000-09-00-0186 Rev A
		Verify that the VT interlock is closed by all faults clear on GUI
		Disconnect VT cable 180101_C1 from feedthrough
		entropy to recommend the property of the prope

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		Han B Fre-rower-Op Interlock Checkout Procedure		
	1	Verify that the fast dump breaker has opened		
	/	Verify that the SOE indicate "VT cable interlock"		
	/	Reconnect cable 180101_C1 from feedthrough		
		Clear the interlock fault on the GUI or "PLC Expert Screen"	1 4/-17	
	/	Repeat the above steps for cables :180101-180110	-77	
		cable 180102		
	/	cable 180103		
	0/1	cable 180104		
< 1 - 549.	/	cable180105		
		cable 180106		
	/	cable180107		
	/	cable180108	247.5	
	1	cable180109		
	V	cable180110		
1/23/2017	TL/PC	Test Hardwire Interlock System Cable Interlock		
job da		Reference DWG B00000-09-00-0162 Rev A, B00000-09-00-0169 Rev A, 0172, B00000-09-00-0178	B00000-09	-00-
		Verify that the System cable interlock is closed by all faults clear indica	ting on GUI	
		Disconnect System cable 162109_A at connector LC817E1,E2		
	V	Verify that the fast dump breaker has opened		
		Verify that the SOE indicate "System Cable Interlock"		
		Reconnect System cable 162109_A at connector LC817E1, E2		
		Clear the interlock fault on the GUI or "PLC Expert Screen"	361 71	
		Repeat the above steps for all system cables:	0	
		cable 162426_A at Connector LC817B3,B4	for	
	sim post	cable 162509_A at connector LC817C1,C2	127-A	
		cable 162526_A at connector LC817C3,C4	8104	
		cable 162609_A at connector LC817D1,D2		
		cable 162626_A at connector LC817D3,D4		
		cable 162709_A at connector LC817H1		
		cable 162726_A at connector LC817H4		
		cable 169141_A at connector 817E1		
		cable 169236_A at connector 817E2		
	- L	cable 169341_A at connector 817E3	24/11	Employ 1
1, 977	-	cable 172108_A at connector 817U1HB1		
		cable 172130_A at connector 817D1HB1		
		cable 172209_A at connector 817U4HB1		
		•		

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Hall B Pre-Power-Up Interlock Checkout Procedure	
cable 17229_A at connector 817D4HB1	
cable 178131_A at connector 8122C	
cable 178231_A at connector 8102	
cable 178331_A at connector 8103	
cable 178427_A at connector 8104	
cable 178531_A at connector 8124	
cable 178631_A at connector 8127	
cable 178731_A at connector 8125	
cabe 178831_A at connector 8128	
March 2017 - Francisco Company and Indicate	
channel Interlock	
/PC Test Danfysik QD Sum1	
Reference B00000-09-00-0180 TORUS Voltage Tap Schematic	
Temporarily disassociate the PLC software interlock tag from control fast dump	olled ramp down and
Test QD Ch 1 by inserting a voltage source at Voltage tap using app	ropriate taps
Slowly raise the voltage in 5mV increments starting at 50mV until t	hreshold is hit
	111 an
Verify that the fast dump breaker has opened	Noto: All aD
Verify that the SOE indicate "QD Sum1 "	tests regard is
Reduce voltage source to 0mV, clear the interlock/reset MPS	tests required ms via board; couldnot reset with EPI
Reverse the voltage source leads and repeat the test	riset with EPI
Record the actual trip threshold - 189 mV	1654 4161-1-
Verify that the fast dump breaker has opened	
✓ Verify that the SOE indicate "QD Sum1 "	
Reduce voltage source to 0mV, clear the interlock/reset MPS	
Test QD Ch 2 by inserting a voltage source at voltage tap test panel appropriate taps	using the
Slowly raise the voltage in 5mV increments starting at 50mV until the	
Record the actual trip threshold + 187 mV	nreshold is hit
	hreshold is hit
Verify that the fast dump breaker has opened	nreshold is hit
Verify that the fast dump breaker has opened Verify that the SOE indicate "QD Sum1 "	hreshold is hit
	hreshold is hit

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Record the actual trip threshold $-189 \,\mathrm{mV}$ Verify that the fast dump breaker has opened

		Han D 11c-10wel-Op Interlock Checkout 1 locedure	
		Verify that the SOE indicate "QD Sum1 "	
		Reduce voltage source to 0mV, clear the interlock/reset MPS	
	1	Test QD Ch 3 by inserting a voltage source at Voltage tap using appr	ropriate taps
	/	Slowly raise the voltage in 5mV increments starting at 50mV until the	
		Record the actual trip threshold + 200 mV	
	-	Verify that the fast dump breaker has opened	
		Verify that the SOE indicate "QD Sum1 "	
	1/	Reduce voltage source to 0mV, clear the interlock/reset MPS	
	V	Reverse the voltage source leads and repeat the test	
	V	Record the actual trip threshold -185 mV	
	~	Verify that the fast dump breaker has opened	
	/	Verify that the SOE indicate "QD Sum1 "	
	~	Reduce voltage source to 0mV, clear the interlock/reset MPS	24/21 1100
	V	Test QD Ch 4 by inserting a voltage source at Voltage tap using appr	opriate taps
		Slowly raise the voltage in 5mV increments starting at 50mV until th	reshold is hit
	~	Record the actual trip threshold + 199 mV	
		Verify that the fast dump breaker has opened	
10	~	Verify that the SOE indicate "QD Sum1 "	
		Reduce voltage source to 0mV, clear the interlock/reset MPS	
b		Reverse the voltage source leads and repeat the test	
270		Record the actual trip threshold -197 mV	
1	/	Verify that the fast dump breaker has opened	
-		Verify that the SOE indicate "QD Sum1 "	
		Reduce voltage source to 0mV, clear the interlock/reset MPS	
		a solve a solve and all the so	
1	TI 100	The second secon	
	11/10	Test Danfysik QD Sum2 Reset the MPS, Refer to B00000-09-00-0180 TORUS Voltage Tap Sch	omatic
	1	Temporarily disassociate the PLC software interlock tag with ramp d	
	1	Test QD Ch 5 by inserting a voltage source at Voltage tap using appro	
		Slowly raise the voltage in 5mV increments starting at 50mV until th	
	,	The control of the co	
	~	Verify that the fast dump breaker has opened	Vote: has to be cost in local MPS control
	~	Verify that the SOE indicate "QD Sum"2"	ia local Mfs control
		Reduce voltage source to 0mV, clear the interlock/reset MPS	Mancy
	./	Reverse the voltage source leads and repeat the test	
		Record the actual trip threshold -213 mV	
	624	necord the actual trip threshold - pro	

1/24/17

/	Verify that the fast dump breaker has opened	
/	Verify that the SOE indicate "QD Sum".	
/	Reduce voltage source to 0mV, clear the interlock/reset MPS	
/	Test QD Ch 6 by inserting a voltage source at voltage tap test panel using the appropriate taps	
V	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit Record the actual trip threshold+ 197 mV	
	Verify that the fast dump breaker has opened	
	Verify that the SOE indicate "QD Sum"	
V	Reduce voltage source to 0mV, clear the interlock/reset MPS	
	Reverse the voltage source leads and repeat the test	
V	Record the actual trip threshold - 208mV	
~	Verify that the fast dump breaker has opened	
~	Verify that the SOE indicate "QD Sum2"	
~	Reduce voltage source to 0mV, clear the interlock/reset MPS	
V	Test QD Ch 7 by inserting a voltage source at Voltage tap using appropriate taps	
V	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit	
V	Record the actual trip threshold + 102 mV	
	Verify that the fast dump breaker has opened	
V	Verify that the SOE indicate "QD Sum"."	
V	Reduce voltage source to 0mV, clear the interlock/reset MPS	
V	Reverse the voltage source leads and repeat the test	
V	Record the actual trip threshold -94 mV	
V	Verify that the fast dump breaker has opened	
~	Verify that the SOE indicate "QD Sum?"	
V	Reduce voltage source to 0mV, clear the interlock/reset MPS	
/	Test QD Ch 8 by inserting a voltage source at Voltage tap using appropriate taps	
V	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit	
_	Record the actual trip threshold $+ 163 \text{mV}$	
V	Verify that the fast dump breaker has opened	
V	Verify that the SOE indicate "QD Suma"	
	Reduce voltage source to 0mV, clear the interlock/reset MPS	
V	Reverse the voltage source leads and repeat the test	
	Record the actual trip threshold - 103 mV	
V	Verify that the fast dump breaker has opened	
V	Verify that the SOE indicate "QD Sum"	
	Reduce voltage source to 0mV, clear the interlock/reset MPS	

129/2017 TL/PC	Test Danfysik QD Sum3	
	Reset the MPS, Refer to B00000-09-00-0180 TORUS Voltage Tap Sche	matic
~	Temporarily disassociate the PLC software interlock tag with ramp do	
	Test QD Ch ${m q}$ by inserting a voltage source at Voltage tap using appro	
V	Slowly raise the voltage in 5mV increments starting at 50mV until three Record the actual trip threshold $+2.16$	
V	Verify that the fast dump breaker has opened	
V	Verify that the SOE indicate "QD Sum?"	-
V	Reduce voltage source to 0mV, clear the interlock/reset MPS	
V	Reverse the voltage source leads and repeat the test	
	Record the actual trip threshold -2.20 V	
	Verify that the fast dump breaker has opened	
	Verify that the SOE indicate "QD Sum3"	
	Reduce voltage source to 0mV, clear the interlock/reset MPS	
	and the state of t	
123/2017 TL/PC	The Mark Control of the Control of t	
12512017 12/PC	Test PLC Fast Dump Button(Epic's GUI	
	Verify all interlocks are clear	
	on the interlock screen depress the fast dump button	
	Click yes when the prompt comes up "are you sure you want to do thi	S"
V	verify that the dump contactor opened	
	Verify that the SOE indicates "PLC fast dump"	W
	In PLC Expert screen verify that the GUI button was the source for ope dump sum	ening the PLC fast
	Reset the MPS, Verify all interlocks are clear	
	New Estate in an amount of many	
	Test PLC Hard coded current limit Verify all interlocks are clear X Not Required	
	In the PLC expert screen disassociate the MPS current tag from the ha	rd coded current
	Insert a test tag with a number greater than 3800A	
	Verify that the dump contactor opened	
	Verify that the SOE indicates "PLC fast dump"	
	verify that the SOL maleates The last dump	

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	pd 7, 4 a	In PLC Expert screen verify that the hard current was the source for opening the PLC fast dump sum
		Reset the MPS, Verify all interlocks are clear
		Test PLC ramp down failure
		Verify all interlocks are clear * Not Required
		In the PLC expert screen disassociate the di/dT tag from the ramp down failure routine
		Insert a test tag with a number less than 2.0A/s
		Initiate a "controlled ramp down" by forcing the sum bit true
	THE R	Verify that the dump contactor opened
		Verify that the SOE indicates "PLC fast dump"
		In PLC Expert screen verify that the ramp down monitor was the source for opening the PLC fast dump sum
		Reset the MPS, Verify all interlocks are clear
	I	Test PLC VESDA fire detection # Nat D
		Test PLC VESDA fire detection
		In the PLC expert screen force the "VESDA" bit true
		Verify that the dump contactor opened
	UET 8	Verify that the SOE indicates "PLC fast dump"
		In PLC Expert screen verify that the VESDA bit was the source for opening the PLC fast dump sum
	pu ille ii	Reset the MPS, Verify all interlocks are clear
		THE THIRD
1/24/2017	TL/PC	Test PLC Software quench, 2nd threshold * Disabled tist
	L	Disable the three hardwire QD sums with "flagged" jumpers Thorshold
		Disable the PLC QD controlled ramp down by temporarily raising the thresholds to 250mV
		Verify that the VT panel is isolated from the magnet checking position of switches
	~	The below steps will be repeated and recorded for each of the ten comparators:
1/24/2017	TL/AC	Comparator 1 * Also disabled
1- (20)	V	Place voltage source1 on VT5-DAQ and set it at 200mV C4, C6, and C7 Place voltage source2 on VT8-DAQ and set it at 80mV
	~	I lade tottebe control of the state of the s
	/	Slowly decrease the voltage on source2 by 5mV increments until you get a trip VTS-DAG
	~	Verify the dump contactor opened
		Verify the SOE indicate "PLC Fast dump

	In PLC Expert screen verify that the PLC QD was dump sum	
_	Record the difference of source 1 and source2	Source 1 = 300 ml
\vdash	Remove both sources	AV = 250 mV
		ALL STREET, ST
	Clear the interlock fault on the GUI or "PLC Expe	
	•	no President (197 grille d
\dashv	Place voltage source1 on VT9-DAQ and set it at	
\dashv	Place voltage source2 on VT12-DAQ and set it a	
\dashv	Slowly decrease the voltage on source2 by 5mV	increments until you get a trip
-	Verify the dump contactor opened	
-	Verify the SOE indicate "PLC Fast dump	THE RESPONSE OF THE
	In PLC Expert screen verify that the PLC QD was dump sum	the source for opening the PLC fast
	Record the difference of source 1 and source2	
	Remove both sources	
	Clear the interlock fault on the GUI or "PLC Expe	ert Screen"
	Comparator 3 * Nort Required	
	Place voltage source1 on VT13-DAQ and set it at	t 200mV
	Place voltage source2 on VT16-DAQ and set it a	t 80mV
	Slowly decrease the voltage on source2 by 5mV	increments until you get a trip
	Verify the dump contactor opened	
	Verify the SOE indicate "PLC Fast dump	
	In PLC Expert screen verify that the PLC QD was dump sum	the source for opening the PLC fast
Jii	Record the difference of source 1 and source2	
0 1	Remove both sources	promise and an experience of the contract of t
- Section 1	Clear the interlock fault on the GUI or "PLC Expe	ert Screen"
UF II	Comparator 4 Not Required	
	Place voltage source1 on VT5-DAQ and set it at 2	200mV
	Place voltage source2 on VT10-DAQ and set it a	t 80mV
	Slowly decrease the voltage on source2 by 5mV	increments until you get a trip
00	Verify the dump contactor opened	1 1000 million 705 711
	Verify the SOE indicate "PLC Fast dump	
	In PLC Expert screen verify that the PLC QD was	the source for opening the PLC fast
4	dump sum	
	Record the difference of source 1 and source2	
J	Remove both sources	

	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 5 X Not Riquird
	Place voltage source1 on VT9-DAQ and set it at 200mV
	Place voltage source2 on VT14-DAQ and set it at 80mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the dump contactor opened
	Verify the SOE indicate "PLC Fast dump
	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	Record the difference of source 1 and source2
	Remove both sources
111% = 1	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 6 * Not Required
	Place voltage source1 on VT13-DAQ and set it at 200mV
2 min	Place voltage source2 on VT6-DAQ and set it at 80mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the dump contactor opened
	Verify the SOE indicate "PLC Fast dump
	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	Record the difference of source 1 and source2
	Remove both sources
m -	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 7 # Not Required
	Place voltage source1 on VT5-DAQ and set it at 200mV
	Place voltage source2 on VT18-DAQ and set it at 80mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
\neg	Verify the dump contactor opened
\neg	Verify the SOE indicate "PLC Fast dump
	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	Record the difference of source 1 and source2
	Remove both sources
\neg	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 8 x NA Regulard
\neg	Place voltage source1 on VT3-DAQ and set it at 200mV
\neg	Place voltage source2 on VT19-DAQ and set it at 80mV

		Slowly decrease the voltage on source2 by 5mV increments until you get a trip
		Verify the dump contactor opened was a such as
		Verify the SOE indicate "PLC Fast dump
		In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast
	1019/101	dump sum
		Record the difference of source 1 and source2
		Remove both sources
	n Dikim	Clear the interlock fault on the GUI or "PLC Expert Screen"
		Place voltage source1 on VT2-DAQ and set it at 200mV
		Place voltage source1 on VT2-DAQ and set it at 200mV
		Place voltage source2 on VT20-DAQ and set it at 80mV
		Slowly decrease the voltage on source2 by 5mV increments until you get a trip
		Verify the dump contactor opened
		Verify the SOE indicate "PLC Fast dump
		In PLC Expert screen verify that the ramp PLC QD was the source for opening the PLC fast dump sum
		Record the difference of source 1 and source2
		Remove both sources
		Clear the interlock fault on the GUI or "PLC Expert Screen"
		A CONTRACTOR OF THE PROPERTY O
		Place voltage source1 on VT1-DAQ and set it at 200mV
		Place voltage source2 on VT21-DAQ and set it at 80mV
		Slowly decrease the voltage on source2 by 5mV increments until you get a trip
		Verify the dump contactor opened
		Verify the SOE indicate "PLC Fast dump
	-6000	In PLC Expert screen verify that the ramp PLC QD was the source for opening the PLC fast dump sum
		Record the difference of source 1 and source2
		Remove both sources
	at CLUF on	Clear the interlock fault on the GUI or "PLC Expert Screen"
	V	Enable the PLC QD controlled ramp down by lowering the thresholds to 100mV
	V	Reinstall the three hardwire QD sums be removing "flagged" jumpers
,		2 in 1997 to 10 of a 40 mile
	TI 60	Clear to sent and the content of the
1/24/2017	V	Test PLC UPS battery low signal Verify all interlocks are clear
	~	In the PLC expert screen force the "PLC UPS battery Low"

X	Verify that the dump contactor opened & Lausis Controlled Ramp down
X	Verify that the SOE indicates "PLC fast dump"
/	In PLC Expert screen verify that the UPS battery Low was the source for opening the PLC fast dump sum
V	Reset the MPS, Verify all interlocks are clear
1	Verify all interlocks are clear
	In the PLC expert screen force the "ESR Fault" bit
	Verify that the dump contactor opened
	In PLC Expert screen verify that the ESR fault was the source for opening the PLC fast dump sum
	Reset the MPS, Verify all interlocks are clear
A A	Verify all interlocks are clear * Not Required
	In the PLC expert screen associate a temporary tag as the Axial SG with a value higher than the current limit
0.0	Verify that the MPS ramp down was initiated via comms routine
	In PLC Expert screen verify that the Axial SG was the source for ramp down sum
	Remove the temporary test tag and re-associate correct tag
	Reset the MPS, Verify all interlocks are clear
	Verify all interlocks are clear Vot Required
	In the PLC expert screen associate a temporary tag as the DS Hex Beam SG with a value higher than the current limit
	Verify that the MPS ramp down was initiated via comms routine
	In PLC Expert screen verify that the DS Hex Beam SG was the source for ramp down sum
	Remove the temporary test tag and re-associate correct tag
	Reset the MPS, Verify all interlocks are clear
1	JS Hex Beam SG Controlled Ramp Down
	Verify all interlocks are clear * Not Required
n	In the PLC expert screen associate a temporary tag as the US Hex Beam SG with a value higher than the current limit
	Verify that the MPS ramp down was initiated via comms routine
	In PLC Expert screen verify that the US Hex Beam SG was the source for ramp down sum
	Remove the temporary test tag and re-associate correct tag

Ling in	Reset the MPS, Verify all interlocks are clear
	CCM Load Cell Controlled Ramp Down * Not Required
geting il	Verify all interlocks are clear
	In the PLC expert screen associate a temporary tag as the CCM Load Cell with a value higher than the current limit
	Verify that the MPS ramp down was initiated via comms routine
	In PLC Expert screen verify that the CCM Load Cell was the source for ramp down sum
	Remove the temporary test tag and re-associate correct tag
	Reset the MPS, Verify all interlocks are clear
	Vertical Support Controlled Ramp Down * NA Required Verify all interlocks are clear
	In the PLC expert screen associate a temporary tag as the Vertical Support with a value higher than the current limit
	Verify that the MPS ramp down was initiated via comms routine
	In PLC Expert screen verify that the Vertical Support was the source for ramp down sum
	Remove the temporary test tag and re-associate correct tag
	Reset the MPS, Verify all interlocks are clear
	Software Quench, 1st threshold Controlled Ramp Down X Not Required, only 21 Disable the three hardwire QD sums with "flagged" jumpers Threshold Chroked
\vdash	Disable the PLC QD fast ramp down by temporarily raising the thresholds to 250mV
\vdash	Verify that the VT panel is isolated from the magnet checking position of switches
	The below steps will be repeated and recorded for each of the ten comparators: Comparator 1 Wot Required
The state of the same	Place voltage source1 on VT5-DAQ and set it at 200mV
	Place voltage source2 on VT8-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	Record the difference of source 1 and source2
	Remove both sources
m may an	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 2 x Not Pequinal
	Place voltage source1 on VT9-DAQ and set it at 200mV
Arold throw	Place voltage source2 on VT12-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip

	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp
	down down
	Record the difference of source 1 and source2
r for Land	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 3 * Not Regulard
	Place voltage source1 on VT13-DAQ and set it at 200mV
	Place voltage source2 on VT16-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp
	down down
	Record the difference of source 1 and source2
	Remove both sources
port aut	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 4 Not Required
	Place voltage source1 on VT5-DAQ and set it at 200mV
	Place voltage source2 on VT10-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
m V as	Record the difference of source 1 and source2
	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
tel sit	Comparator 5 X Not Required
	Place voltage source1 on VT9-DAQ and set it at 200mV
	Place voltage source2 on VT14-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	Record the difference of source 1 and source2
net st	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 6 * Not Regained

	Place voltage source1 on VT13-DAQ and set it at 200mV
a not set	Place voltage source2 on VT6-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	Record the difference of source 1 and source2
	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
(151 F	Comparator 7 * Not Require
	Place voltage source1 on VT5-DAQ and set it at 200mV
1 lobilemi	Place voltage source2 on VT18-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the dump contactor opened
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	Record the difference of source 1 and source2
	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
	Comparator 8 * Not Required
	Place voltage source1 on VT3-DAQ and set it at 200mV
a see a see	Place voltage source2 on VT19-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the dump contactor opened
	Verify the Fast Ramp Down was initiated
	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	Record the difference of source 1 and source2
darad	Remove both sources
	Clear the interlock fault on the GUI or "PLC Expert Screen"
e ii al ada	Comparator 9 * Not Required
	Place voltage source1 on VT2-DAQ and set it at 200mV
	Place voltage source2 on VT20-DAQ and set it at 120mV
	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	Verify the dump contactor opened
	Verify the Fast Ramp Down was initiated
	a symptom while a

		In PLC Expert screen verify that the ramp PLC QD was the source for in ramp down	itiating the fast
		Record the difference of source 1 and source2	
-		Remove both sources	
		Clear the interlock fault on the GUI or "PLC Expert Screen"	
	Cor	mparator 10 * Not Required	
		Place voltage source1 on VT1-DAQ and set it at 200mV	
	- 10	Place voltage source2 on VT21-DAQ and set it at 120mV	
2 Samples	Local Co.	Slowly decrease the voltage on source2 by 5mV increments until you go	et a trip
2 0	Man on	Verify the Fast Ramp Down was initiated	
	ون	In PLC Expert screen verify that the ramp PLC QD was the source for ini ramp down	tiating the fast
		Record the difference of source 1 and source2	
		Remove both sources	
		Clear the interlock fault on the GUI or "PLC Expert Screen"	
	- 10	Enable the PLC QD controlled ramp down by lowering the thresholds to	100mV
		Reinstall the three hardwire QD sums be removing "flagged" jumpers	
	2 1		
1/14/2017 Th	/PC Vac	cuum Interlock Controlled Ramp Down	
100		Verify all interlocks are clear	
L		In the PLC expert screen force associate a temporary test tag to the vac	cuum interlock
L		In the PLC expert screen force associate a temporary test tag to the vac and raise the value above threshold Verify the Fast Ramp Down was initiated	
L V		In the PLC expert screen force associate a temporary test tag to the vac	
L		In the PLC expert screen force associate a temporary test tag to the vacuum draise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating	
L N		In the PLC expert screen force associate a temporary test tag to the vacuum description of the vacuum was the source for initiating ramp down	
L	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuum raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear	
L N	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuand raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear	
L N	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuum raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiatin ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear C's WatchDog Controlled Ramp Down **Not Regard **Reset the MPS in the correct tag **Reset tag tag tag tag tag tag tag tag tag ta	
	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuum raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear C's WatchDog Controlled Ramp Down Verify all interlocks are clear	
	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuand raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear C's WatchDog Controlled Ramp Down Verify all interlocks are clear In the EPICS expert screen force stop on the heartbeat	g the PLC fast
	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuand raise the value above threshold Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiating ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear C's WatchDog Controlled Ramp Down Verify all interlocks are clear In the EPICS expert screen force stop on the heartbeat Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the EPIC's Watchdog was the source for	g the PLC fast
	EPIC	In the PLC expert screen force associate a temporary test tag to the vacuand raise the value above threshold Verify the fast Ramp Down was initiated In PLC Expert screen verify that the vacuum was the source for initiatin ramp down Remove test tag and re-associate the correct tag Reset the MPS, Verify all interlocks are clear C's WatchDog Controlled Ramp Down Verify all interlocks are clear In the EPICS expert screen force stop on the heartbeat Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the EPIC's Watchdog was the source for fast ramp down	g the PLC fast

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		op menden energet i totture
		Verify all interlocks are clear
	V	Lower the pinterlock threshold to 1.9ATM
		Verify the Fast-Ramp Down was initiated
	V	In PLC Expert screen verify that the Helium Pressure interlock was the source for initiating the fast ramp down
	V	Raise the helium pressure interlock back to 2.5ATM
	V	Reset the MPS, Verify all interlocks are clear
1/24/2017	TL/8C	Nitrogen Pressure Controlled Ramp Down (requires at least 1.0ATM of nitrogen)
() Firm	1	
		Verify all interlocks are clear Lower the interlock threshold to 0.5ATM Verify the Fast Ramp Down was initiated * Did not change parameters, tripped on aum as testing
	/	In PLC Expert screen verify that the Nitrogen Pressure interlock was the source for initiating the fast ramp down
	~	Raise the nitrogen pressure interlock back to 0.9ATM
		Reset the MPS, Verify all interlocks are clear
	V-3000	Nitrogen Pressure Controlled Ramp Down (requires at least 1.0ATM of nitrogen)
		Verify all Interlocks are clear
		Lower the interlock threshold to 0.5ATM
		Verify the Fast Ramp Down was initiated # Duplicate of 900 VC
	lis Ini mi	In PLC Expert screen verify that the Nitrogen Pressure interlock was the source for initiating the fast ramp down
		Raise the nitrogen pressure interlock back to 0.9ATM
		Reset the MPS, Verify all interlocks are clear
124/2017	TL/AC	Lhe Liquid Level Controlled Ramp Down Lower(requires at least 20% helium)
	~	Verify all interlocks are clear
	_	Raise the interlock threshold to 22%
		Verify the Fast Ramp Down was initiated
		In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
		Return the Lhe LL interlock back to 20%
	~	Reset the MPS, Verify all interlocks are clear
124/2017	TL/PC	Lhe Liquid Level Controlled Ramp Down Upper (requires at least 20% helium)
		Verify all interlocks are clear
	V	Lower the interlock threshold to 18% Centralise Verify the Fast Ramp Down was initiated
		inputed in admission of the control

	In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
or the miles	Raise the Lhe LL interlock back to 90%
	Reset the MPS, Verify all interlocks are clear
a a. (Francis)	LN2 Liquid Level Controlled Ramp Down Lower (requires at least 20% helium) Verify all interlocks are clear Raise the interlock threshold to 22% Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
	Return the Lhe LL interlock back to 20%
	Reset the MPS, Verify all interlocks are clear
	LN2 Liquid Level Controlled Ramp Down Upper(requires at least 20% helium) * Not Required, Verify all interlocks are clear Lower the interlock threshold to 18% Af PLC code
	Verify the Fast Ramp Down was initiated In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
turnetand.	Return the Lhe LL interlock back to 90% Reset the MPS, Verify all interlocks are clear
1/24/2017 TL/PC	Verify interlocks to prevent over-current Verify code does not allow user to enter current higher than planned in procedure
~	Verify code triggers a controlled discharge if current limit is exceeded
~	Verify hardware limit in power supply is set to maximum current expected during procedure
N	The Call of Part of the Control of t

Checks to be performed prior to full-current operation

Depending on time elapsed between low-current and full-current operations, repeat some of the pre-checks that are deemed necessary to resume operations. In addition, the following checks are to be completed prior to full-current operation (or could happen in parallel to low-current operations).

-{veck 2 Deck	Verify that interlocks for magnet mechanical monitoring are finalized (spi operational	readsheet) and
	Verify interlocks for support forces	
i gettreft	Verify interlocks for hex-beam forces	
	Verify interlocks for hub forces	
	Verify interlocks for combined load scenarios	

1/24/2017

Note: During testing, in Cryo Cantrolled Ramp Pown interlock K-pt tripply on VCL Flow and No overpressure

· VCL flow ranged from 28 slm to 90 slm, lower limit = 73.5 slm.

. No pressor ronged from 2.20 Atm to 2.40 atm; tower!

Overpressore limit = 2.25 atm.

Note:

VX is the derived parameters and VTXX_DAQ (defined as in DRG B00000-09-00-180):

```
V1 := (VT5 DAQ + VT6 DAQ + VT7 DAQ);//VOLTS//S3 + Coil A + S10
V2 := (VT7 DAQ + VT8 DAQ + VT9 DAQ);//VOLTS//S4 + Coil B + S3
V3 := (VT9 DAQ + VT10 DAQ + VT11 DAQ);//VOLTS//S4 + Coil C + S5
V4 := (VT11 DAQ + VT12 DAQ + VT13 DAQ);//VOLTS//S6 + Coil D + S5
V5 := (VT13 DAQ + VT14 DAQ + VT15_DAQ);//VOLTS//S1 + Coil E + S6
V6 := (VT15 DAQ + VT16 DAQ + VT17 DAQ);//VOLTS//S1 + Coil F + (S7 + S2)//Lead
In resistive voltages
V7 := (VT5 DAQ + VT4 DAQ + VT3 DAQ);//VOLTS//S10 + Vac break in +
Lead Ext In
V8 := (VT3_DAQ);//VOLTS//S9 + Lead_Ext_In
V9 := (VT2 DAQ);//VOLTS//Lead Ext solder joint @ vcl cold end IN
V10 := (VT1 DAQ);//VOLTS//VCL In
V16 := (VT1 DAQ + VT2 DAQ + VT3 DAQ + VT4 DAQ + VT5 DAQ);//VOLTS// Resistive
section IN
//whole magnet V11 := VT22 DAQ;//VOLTS//Whole magnet RT lead to lead
//V18 := VTXX DAQ/1000000;//VOLT//Whole magnet 4.2K lead to lead
VTXX DAQ: VT2 DAQ + VT3 DAQ + VT4 DAQ + VT5 DAQ + VT6 DAQ + VT7 DAQ + VT8 DAQ
+ VT9_DAQ + VT10_DAQ + VT11_DAQ + VT12_DAQ + VT13_DAQ + VT14_DAQ + VT15_DAQ +
VT16_DAQ + VT17_DAQ + VT18_DAQ + VT19_DAQ + VT20_DAQ
//Lead Out resistive voltages
V12 := (VT21 DAQ);//VOLTS//VCL Out
V13 := (VT20_DAQ);//VOLTS//Lead ext solder joint @ vcl cold end OUT
V14 := (VT19 DAQ);//VOLTS//S8 + Lead_Ext_Out
V15 := (VT17_DAQ + VT18_DAQ + VT19_DAQ);//VOLTS//(S7 + S2) + Vac Break OUT +
Lead Ext OUT
V17 := (VT17 DAQ + VT18 DAQ + VT19 DAQ + VT20 DAQ + VT21_DAQ);//VOLTS
// Resistive section out
```