**Torus FastDAQ Time Gaps**

**Date: February 01, 2017**

**Time: 9:30 – 10:15**

*Attendees: Nathan Baltzell, Pablo Campero, Ruben Fair, Tyler Lemon, Wesley Moore*

1. Three types of “time gaps” seen in recorded FastDAQ data.
	1. “Time gap” defined as any length of time where FastDAQ data is recorded as zero when there should be data.
	2. Time gaps only seen in recorded FastDAQ data.
	3. Three types of time gaps: random jitter, 200 [ms] gaps, EPICS timestamp skew.
2. Tim Gap 1: random jitter
	1. Inherent in data acquisition system
	2. Caused by cRIO data acquisition loop not always taking exactly 200ms to execute.
	3. Loop execution times appear to form Gaussian distribution centered at 200 [ms] and ranging from 190 [ms] – 210 [ms]
3. Time Gap 2: 200 [ms] gap
	1. 200 [ms] is exact time for one sample acquisition (cRIO updates EPICS at 5 [Hz]).
	2. Also appeared in Fall 2016 during full-current commissioning.
	3. Exact cause of 200 [ms] gaps unknown.
	4. Potential causes:
		1. High cRIO CPU load.
		2. EPICS softIOC gateway bogged down by EPICS Live FastDAQ screen and data recording.
	5. Solution:
		1. Wesley Moore contacted Christiana Wilson to ask if she found solution in Fall 2016.
		2. Nathan Baltzell or Wesley Moore will disable EPICS Live FastDAQ screen so cRIO IOC is only communicating with data logger.
4. Time Gap 3: EPICS timestamp skew.
	1. EPICS timestamps for all voltage taps not identical.
	2. Having identical timestamps for voltage taps critical to troubleshooting any quench event.
	3. Caused by data written at different times by cRIO to shared variables used to pass data to EPICS.
	4. Solution:
		1. Tyler Lemon will determine which voltage tap is sent to EPICS first.
		2. Nathan Baltzell will use voltage tap sent to EPICS first as “master timestamp” and give all other voltage taps the master timestamp.