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| TITLE: **Hall B Solenoid Pre-Power-Up Interlock Checkout Procedure (DRAFT)** |

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| BY: Pablo Campero | DATE: 01 / 25 / 2017 |
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| REV. | ECO# | DESCRIPTION | BY | CHK. | APP. | APP. | DATE |
| SUMMARY OF CHANGES FROM PREVIOUS REVISION: | | | | | | | | |

Goals – Ensure Solenoid magnet interlock systems are operational prior to powered-up operation (some need to be checked prior to low-current operation, all need to be complete prior to full-current operation)

1. Perform all interlock checks. Some require the magnet to be full of liquid helium.
2. Prior to perform any task of the current list makes sure that all the interlocks are clear. Verify on Fast Dump, MPS Internal and PLC Controlled Ramp Down interlocks status screens display clear (green indicators) on EPICS.

Administrative Requirements

During and after cooldown, complete the appropriate items in Pre Power Up interlock Checklist below. Upload a copy of the completed checklist to the Solenoid Electronic Logbook.

<https://logbooks.jlab.org/book/hbsolenoid>

**Checks to be performed prior to injecting current to magnet (low-current operation)**

***PLC Hardware Interlock***

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|  | **Test Hardwire interlock PLC Chassis watchdog** | |  |
|  |  | Reset the MPS, and use reference DWG B00000-09-00-0653 and B00000-09-00-0645. |  |
|  |  | Remove Timer Relay TYCO CNT-35-96 from DIN socket, wait 5 seconds. |  |
|  |  | Verify that the fast dump breaker has opened. |  |
|  |  | Verify that the SOE indicates “PLC Chassis Watchdog”. |  |
|  |  | Reinstall Timer Relay TYCO CNT-35-96 into DIN socket, wait 30 seconds. |  |
|  |  | Clear the interlock fault on the GUI or “PLC Expert Screen”. |  |
|  | **Test Hardwire Interlock Current lead water flow (1.4GPM switch)** (Solenoid has the same switches as MPS Torus?) | |  |
|  |  | Reset the MPS. Use reference DWG B00000-09-00-0660 and B00000-09-00-0645. | |
|  |  | Verify the current lead flow switch circuit is closed. |  |
|  |  | Verify that water is flowing through the current leads. |  |
|  |  | Temporarily jumper across the 1.2 GPM switch, Wire 660450. |  |
|  |  | Slowly close the current lead water supply valve. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE indicate “Current Lead Water Flow”. |  |
|  |  | Unjumper the wire across the 1.2 GPM switch. |  |
|  |  | Slowly open the current lead water supply valve. |  |
|  |  | Clear the interlock fault on the GUI (MPS Control screen) or “PLC Expert Screen”. |  |
|  | **Test Hardwire Interlock Current lead water flow (1.2GPM switch)** (same switches as Torus?) | |  |
|  |  | Reset the MPS. Use Reference DWG B00000-09-00-0660. | |
|  |  | Verify the current lead flow switch circuit is closed. |  |
|  |  | Verify that water is flowing through the current leads. |  |
|  |  | Temporarily jumper across the 1.4 GPM switch, Wire 660450. |  |
|  |  | Slowly close the current lead water supply valve. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE indicate “Current Lead Water Flow”. |  |
|  |  | Remove the jumper on the wire across the 1.4 GPM switch. |  |
|  |  | Slowly open the current lead water supply valve. |  |
|  |  | Clear the interlock fault on the GUI (MPS Control screen) or “PLC Expert Screen”. |  |
|  | **Test Hardwire Interlock VT Cable Interlock** | |  |
|  |  | Reset the MPS. Use reference DWG B00000-09-00-0686. | |
|  |  | Verify that the VT interlock is closed by all faults clear on GUI. |  |
|  |  | Disconnect VT cable 680101\_C1 from feedthrough. |  |
|  |  | Verify that the fast dump breaker has opened. |  |
|  |  | Verify that the SOE indicate "VT Cable Interlock". |  |
|  |  | Reconnect cable 680101\_C1 from feedthrough. |  |
|  |  | Clear the interlock fault on the GUI (MPS Control screen) or “PLC Expert Screen”. |  |
|  |  | Repeat the above steps for cables: 680101-680109. |  |
|  |  | Cable 680101\_C2. |  |
|  |  | Cable 680102\_C. |  |
|  |  | Cable 680103\_C. |  |
|  |  | Cable 680104\_C1, Cable 680104\_C2. |  |
|  |  | Cable 680105\_C. |  |
|  |  | Cable 680106\_C, Cable 680106\_C2, Cable 680106\_C3. |  |
|  |  | Cable 680107\_C. |  |
|  |  | Cable 680108\_C1, Cable 680108\_C2. |  |
|  |  | Cable 680109\_C. |  |
|  | **Test Hardwire Interlock System Cable Interlock** | |  |
|  |  | Use reference DWG B00000-09-00-0662, B00000-09-00-0665, B00000-09-00-0666, B00000-09-00-0667, B00000-09-00-0668, B00000-09-00-0669, and B00000-09-00-0678. |  |
|  |  | Verify that the System cable interlock is closed by all faults clear indicating on GUI (MPS- Control screen). |  |
|  |  | Disconnect System cable 662109\_A at connector LC867-1. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE indicate "System Cable Interlock". |  |
|  |  | Reconnect System cable 662109\_A at connector LC867-1. |  |
|  |  | Clear the interlock fault on the GUI (MPS Control screen) or “PLC Expert Screen”. |  |
|  |  | Repeat the above steps for all system cables (Cable Interlock): |  |
|  |  | Cable 662126\_A at Connector LC867-2. |  |
|  |  | Cable 662209\_A at connector LC867-3. |  |
|  |  | Cable 662226\_A at connector LC867-4. |  |
|  |  | Cable 662309\_A at connector LC867-5. |  |
|  |  | Cable 662326\_A at connector LC867-6. |  |
|  |  | Cable 662409\_A at connector LC867-7. |  |
|  |  | Cable 662426\_A at connector LC867-8. |  |
|  |  | Cable 665141\_A at connector FT01-1. |  |
|  |  | Cable 666141\_A at connector FT02-1. |  |
|  |  | Cable 667141\_A at connector FT03-1. |  |
|  |  | Cable 668141\_A at connector FT04-1. |  |
|  |  | Cable 669141\_A at connector FT05-1. |  |
|  |  | Cable 678131\_A at connector 8622B. |  |
|  |  | Cable 678231\_A at connector 8602. |  |
|  |  | Cable 678331\_A at connector 8603. |  |
|  |  | Cable 678531\_A at connector 8604. |  |
|  |  | Cable 678527\_A at connector bulkhead?(No assigned name for feedthrough dwg0678) |  |

**QD channel Interlock**

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|  | **Test Danfysik QD Sum1** | |  |
|  |  | Use reference DWG B00000-09-00-0680 Solenoid Voltage Tap Schematic and DWG B00000-00-09-0687 Quench Detectors wiring. |  |
|  |  | Temporarily disassociate the PLC software interlock tag from Controlled Ramp Down and Fast Dump. |  |
|  |  | Test QD Ch 1 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5mV increments starting at 50 mV until threshold will be hit |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0 mV; clear all the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 2 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5mV increments starting at 50 mV until threshold will be hit |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1 ". |  |
|  |  | Reduce voltage source to 0mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 3 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold is hit. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 4 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold will be hit. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1" |  |
|  |  | Reduce voltage source to 0mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum1". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |

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|  | **Test Danfysik QD Sum2** | |  |
|  |  | Use reference DWG B00000-09-00-0680 Solenoid Voltage Tap Schematic and DWG. B00000-00-09-0687 Quench Detectors wiring. |  |
|  |  | Temporarily disassociate the PLC software interlock tag from Controlled Ramp Down and Fast Dump. | |
|  |  | Test QD Ch 5 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold will be hit |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear all the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 6 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold will be hit |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 7 by inserting a voltage source at Voltage Tap panel, use the appropriate taps |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold will be hit. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0mV, clear the interlock/reset MPS. |  |
|  |  | Test QD Ch 8 by inserting a voltage source at Voltage Tap panel, use appropriate taps. |  |
|  |  | Slowly raise the voltage in 5 mV increments starting at 50 mV until threshold will be hit. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |
|  |  | Reverse the voltage source leads and repeat the same steps mentioned above. |  |
|  |  | Record the actual trip threshold. |  |
|  |  | Verify that the fast dump breaker has opened on the MPS. |  |
|  |  | Verify that the SOE and Solenoid Interlock status screen indicate "QD Sum2". |  |
|  |  | Reduce voltage source to 0 mV, clear the interlock/reset MPS. |  |

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|  | **Test PLC Fast Dump Button(Epic's GUI)** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | On the Solenoid MPS Control screen depress the “Fast Dump” button. |  |
|  |  | Click yes when the prompt comes up asking "are you sure you want to do this". |  |
|  |  | Verify that the fast dump contactor has opened on the MPS. |  |
|  |  | Verify that the SOE indicates "PLC fast dump". |  |
|  |  | Verify that the Fast Dump Interlocks screen indicates “EPICS Fast Dump”. |  |
|  |  | In PLC Expert screen verify that the GUI button was the source for opening the PLC fast dump sum. |  |
|  |  | Reset the MPS, verify all interlocks are clear. |  |

Noticed that there is no assigned a interlock task to test the Liquid He Level that is the responsible to generate FAST DUMP in the Torus procedure P027.

Do we need to test this for the Solenoid? Since we have already the LL Helium (LL8620SC) signal connected to the SOE module to generate a FAST DUMP

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|  | **Test PLC Hard coded current limit** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen disassociate the MPS current tag from the hard coded current limit. |  |
|  |  | Insert a test tag with a number greater than **2400A.** |  |
|  |  | Verify that the fast dump contactor has opened on the MPS. |  |
|  |  | Verify that the SOE indicates "PLC fast dump". |  |
|  |  | Verify on GUI that Fast Dum Interlocks screen indicates “Current Limit” tripped. |  |
|  |  | In PLC Expert screen verify that the hard current was the source for opening the PLC Fast Dump Sum. |  |
|  |  | Reset the MPS, verify all interlocks are clear. |  |
|  | **Test PLC Controlled Ramp Down failure** Not interlocked for Torus? Will it be this considered a warning signal for the Solenoid too? | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen disassociate the dI/dt tag from the RampDown\_Monitor routine | |
|  |  | Insert a temporary tag with a number less than 2.5 A/s. |  |
|  |  | Initiate a "PLC Fast Dump" by forcing the “Ramp to Zero” bit true. |  |
|  |  | Verify that a PLC Fast Dump will be generated. |  |
|  |  | Verify that the dump contactor has been opened on the MPS. |  |
|  |  | Verify that the SOE module and GUI(Interlocks status screen) indicate "PLC Fast Dump". |  |
|  |  | In PLC Expert screen verify that the Ramp Down Fail was the source for opening the PLC fast dump sum. |  |
|  |  | Reset the MPS, Verify all interlocks are clear. |  |

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|  | **Test PLC VESDA fire detection** This signal will generate a Controlled Ramp Down or a Fast Dump? | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen force the VESDA or "EPICS\_FIRE" bit true. |  |
|  |  | Verify that the dump contactor has been opened. |  |
|  |  | Verify that the SOE and Interlocks Status screen indicates "PLC Fast Dump". |  |
|  |  | In PLC Expert screen verify that the VESDA (EPICS\_FIRE) bit was the source for opening the PLC Fast Dump Sum. |  |
|  |  | Reset the MPS, Verify all interlocks are clear. |  |

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|  | | | **Test PLC Software quench, 2nd threshold** | |  |
|  | | |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  | | |  | Disable the two hardwire Quench Detectors Sums with "flagged" jumpers at the hardware relays that go to the SOE, use reference DWG B00000-00-09-0645 and 0687. |  |
|  | | |  | Disable the PLC Soft\_Quench (used for 1st threshold) bit that generates a Controlled Ramp Down by using a temporary tag on Software\_Quench\_1st PLC routine. |  |
|  | | |  | Verify that the VT panel is isolated from the magnet checking position of switches. |  |
|  | | |  | The below steps will be repeated and recorded for each of the ten comparators: |  |
|  | | | Comparator 1 For all comparator. Which VTX\_DAQ will we use to inject the voltage across on VT panel? | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. (It could be VT5\_DAQ ? ) |  |
|  | | |  | Place voltage source 2 on VT?\_DAQ and set it at 40 mV. (It could be VT13\_DAQ?) |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump” |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI(MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 2 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. (It could be VT7\_DAQ ? ) |  |
|  | | |  | Place voltage source 2 on VT?\_DAQ and set it at 40mV. (It could be VT11\_DAQ ? ) |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increment the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI(MPS- Control) or “PLC Expert Screen”. |  |
|  | | | For COMP 3,4,5,6,7 and 8 Will be required inject voltage in two taps VTX\_DAQ on the VT panel?  Comparator 3 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. (COMP3 = V3 = VT5\_DAQ + VT6\_DAQ + VT7\_DAQ + VT8\_DAQ ) |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ ? |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI(MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 4 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 5 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 6 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 7 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 8 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. |  |
|  | | |  | ~~Place voltage source 2 on VT?\_DAQ and set it at 40mV.~~ |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 9 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. (It could be VT6\_DAQ ? ) |  |
|  | | |  | Place voltage source 2 on VT?\_DAQ and set it at 40mV. (It could be VT14\_DAQ ? ) |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | | | Comparator 10 | |  |
|  | | |  | Place voltage source 1 on VT?\_DAQ and set it at 100mV. (It could be VT18\_DAQ ? ) |  |
|  | | |  | Place voltage source 2 on VT?\_DAQ and set it at 40mV. (It could be VT12\_DAQ ? ) |  |
|  | | |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get a trip. |  |
|  | | |  | Verify the dump contactor has been opened in the MPS. |  |
|  | | |  | Verify the SOE module indicate "PLC Fast Dump”. |  |
|  | | |  | Verify that the Fast Dump Interlocks Status screen indicate “SW Quench, 2nd Threshold”. |  |
|  | | |  | In PLC Expert screen verify that the PLC QD was the source for opening the PLC Fast Dump Sum. |  |
|  | | |  | Record the difference of source 1 and source 2. |  |
|  | | |  | Remove both sources. |  |
|  | | |  | Reset MPS- clear the interlock fault on the GUI(MPS- Control) or “PLC Expert Screen”. |  |
|  | | |  | Enable the PLC QD Controlled Ramp Down by removing the temporary tag on Software\_Quench\_1st PLC routine. |  |
|  | | |  | Reinstall the three hardwire QD sums by removing "flagged" jumpers. |  |
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| --- | --- | --- | --- |
|  | **Test PLC UPS battery low signal** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen force the "UPS Batt LOW” bit by using a temporary tag. |  |
|  |  | Wait 60 seconds and verify that UPS\_Battery\_Low bit is active. |  |
|  |  | In PLC Expert screen verify that the UPS battery Low was the source for opening the PLC Controlled Ramp Down. |  |
|  |  | Verify that trip for “UPS Battery Low” appears on the PLC Controlled Ramp Down screen. |  |
|  |  | Reset the MPS, and verify all interlocks are clear. |  |

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|  | **Test ESR (End Station Refrigerator Fault)** This signal appears as not interlocked (Only Warning) for Torus. Will we take the same condition for the Solenoid? | |  |
|  |  | Verify all interlocks and warnings are clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen force the "ESR\_INTLCK" bit by associating a temporary tag on the Overhead routine. |  |
|  |  | In PLC Expert screen verify that the ESR fault was the source for having the trip on the Solenoid Interlock Status screen at section of the Warmings (Not Interlocked). |  |
|  |  | Reset the MPS, and verify all interlocks are clear. |  |

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|  | **Load Cell Controlled Ramp Down** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the PLC expert screen associate a temporary tag as the CCM Load Cell with a value higher than the current limit. Do we need to test for the 16 LC axials and Radials? |  |
|  |  | Verify that the MPS ramp down was initiated. |  |
|  |  | In PLC Expert screen verify that the CCM Load Cell was the source to starts a Controlled Ramp Down. | |
|  |  | Verify that trip for “Load Cell” appears on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. |  |
|  |  | Remove the temporary test tag and re-associate correct tag. |  |
|  |  | Reset the MPS, Verify all interlocks are clear. |  |

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|  | **Software Quench, 1st threshold Controlled Ramp Down** | |  |
|  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | Disable the two hardwire Quench Detectors Sums with "flagged" jumpers at the hardware relays that go to the SOE, use reference DWG B00000-00-09-0645 and -0687. |  |
|  |  | Disable the PLC Soft\_Quench\_2nd (used for 2nd threshold) bit that generates a Fast Dump by using a temporary tag on Software\_Quench\_2nd PLC routine. | |
|  |  | Verify that the VT panel is isolated from the magnet checking position of switches. |  |
|  |  | The below steps will be repeated and recorded for each of the ten comparators: |  |
|  | Comparator 1 For all comparator. Which VTX\_DAQ will we use to inject the voltage across on VT panel? | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 m. (It could be VT5\_DAQ ? ) |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. (It could be VT13\_DAQ ? ) |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 2 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | For COMP 3, 4, 5, 6, 7 and 8 Will be required inject voltage in two taps VTX\_DAQ on the VT panel?  Comparator 3 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 4 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 5 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 6 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 7 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 8 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 9 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI(MPS- Control) or “PLC Expert Screen”. |  |
|  | Comparator 10 | |  |
|  |  | Place voltage source 1 on VT?\_DAQ and set it at 100 mV. |  |
|  |  | Place voltage source2 on VT?\_DAQ and set it at 70 mV. |  |
|  |  | Slowly decrease the voltage on source 2 by 5 mV to increments the differential of voltage between the two taps until you get the trip. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | In PLC Expert screen verify that the PLC QD was the source for initiating the Controlled Ramp Down. |  |
|  |  | Record the difference of source 1 and source 2. |  |
|  |  | Remove both sources. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  |  | Enable the PLC QD Fast Dump by removing the temporary tag on Software\_Quench\_2nd PLC routine. |  |
|  |  | Reinstall the three hardwire QD sums be removing "flagged" jumpers. |  |

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|  | **Vacuum Interlock Controlled Ramp Down** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). |  |
|  |  | In the “PLC expert screen” associate a temporary test tag to the vacuum interlock and force to raise the value above threshold established. |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | Verify that trip for “Vacuum” appears on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. |  |
|  |  | In “PLC Expert screen” verify that the vacuum was the source for initiating the PLC Controlled Ramp Down. |  |
|  |  | Remove the temporary test tag and re-associate the correct tag on “PLC expert screen”. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. |  |
|  | **EPIC's WatchDog Controlled Ramp Down** | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen) |  |
|  |  | In the “PLC expert screen” associate a temporary test tag to force the EPICS\_Heartbeat |  |
|  |  | Verify the Controlled Ramp Down was initiated. |  |
|  |  | Verify that trip for “EPICS Watchdog” appears on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. |  |
|  |  | In PLC Expert screen verify that the EPIC's Watchdog was the source for initiating the PLC Controlled Ramp Down. |  |
|  |  | Re-enable EPIC's heartbeat by removing the temporary test tag and re-associate the correct tag on “PLC expert screen”. |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI(MPS- Control) or “PLC Expert Screen”. |  |

**Cryogenics Control**

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|  | **Helium Pressure Controlled Ramp Down – Lead Reservoir (Normal range 1.1-1.3 [Atm])**  Do we need to have an interlock task to check the low pressure (Under Pressure) in the Tanks? | | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | In the “PLC Expert screen” lower the helium pressure interlock threshold until it hits a value bellow of the actual pressure reading in PT8620. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the Helium Pressure interlock was the source for initiating the Controlled Ramp Down. | |  |
|  |  | Rerun the helium pressure interlock back to 1.6 [Atm]. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. | |  |
|  | **Helium Pressure Controlled Ramp Down – Magnet Reservoir (Normal Range 0.5-1.2 [Atm])** | | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | In the “PLC Expert screen” lower the helium pressure interlock threshold until it hits a value bellow of the actual pressure reading in PT8670. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the Helium Pressure interlock was the source for initiating the Controlled Ramp Down. | |  |
|  |  | Return the helium pressure interlock threshold back to 1.6 [Atm]. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. | |  |
|  | **LHe Liquid Level Controlled Ramp Down Lower - Lead Reservoir (requires at least 40% of Helium)** | | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen) | |  |
|  |  | In the “PLC Expert screen” raise the Helium Liquid Level Low Interlock threshold until it hits a value above of the actual reading of the liquid level for LL8620DP and LL8620SC. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the LHe Under Limit interlock was the source for initiating the Controlled Ramp Down. | |  |
|  |  | Return the LHe LL interlock threshold back to 40%. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. | |  |
|  | **LHe Liquid Level Controlled Ramp Down Upper - Lead Reservoir**  Do we need to have an interlock task to check the LHe LL High (OverLimit) in the Tanks?If so what would be its threshold? | |  |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | In the “PLC Expert screen” lower the Helium Liquid Level High Interlock threshold until it hits a value bellow of the actual reading of the liquid level LL8620DP and LL8620SC. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the LHe LL High interlock was the source for initiating the Controlled Ramp Down. | |  |
|  |  | Return the LHe LL High interlock threshold back to XX?%. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. | |  |
|  | **LHe Liquid Level Controlled Ramp Down Lower - Magnet Reservoir (requires at least 60% helium)** | | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | In the “PLC Expert screen” raise the Helium Liquid Level Low Interlock threshold until it hits a value above of the actual reading of the liquid level LL8670DP. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the LHe under limit interlock was the source for initiating the Controlled Ramp Down. | |  |
|  |  | Return the LHe Low interlock threshold back to 60%. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI(MPS- Control) or “PLC Expert Screen” | |  |
|  | **LHe Liquid Level Controlled Ramp Down Lower- Magnet Reservoir (requires at least 30% helium)** | | |  |
|  |  | Verify all interlocks are clear by checking all faults clear in GUI (MPS-Interlocks screen). | |  |
|  |  | In the “PLC Expert screen” raise the Helium Liquid Level Low Interlock threshold until it hits a value above of the actual reading of the liquid level for LL8670DP. | |  |
|  |  | Verify the Controlled Ramp Down was initiated. | |  |
|  |  | Verify that trip for “Cryo” displays on the MPS-Interlocks Status screen at the section of the PLC Controlled Ramp Down. | |  |
|  |  | In PLC Expert screen verify that the LHe under limit interlock was the source for initiating the Controlled Ramp Down. | | |
|  |  | Return the LHe Low interlock threshold back to 30%. | |  |
|  |  | Reset PLC Interlocks - Clear interlocks on the GUI (MPS- Control) or “PLC Expert Screen”. | |  |
|  | **Verify interlocks to prevent over-current** | | |  |
|  |  | Verify code does not allow user to enter current higher than planned in procedure. | |  |
|  |  | Verify code triggers a controlled discharge if current limit is exceeded. | |  |
|  |  | Verify hardware limit in power supply is set to maximum current expected during procedure. | |  |

**Checks to be performed prior to full-current operation**

Depending on time elapsed between low-current and full-current operations, repeat some of the pre-checks that are deemed necessary to resume operations. ~~In addition, the following checks are to be completed prior to full-current operation (or could happen in parallel to low-current operations).~~

|  |  |  |  |
| --- | --- | --- | --- |
|  | ~~Verify that interlocks for magnet mechanical monitoring are finalized (spreadsheet) and operational~~ | |  |
|  |  | ~~Verify interlocks for support forces~~ |  |
|  |  | ~~Verify interlocks for hex-beam forces~~ |  |
|  |  | ~~Verify interlocks for hub forces~~ |  |
|  |  | ~~Verify interlocks for combined load scenarios~~ |  |

**Note:**

**VX is the derived parameters and VTXX\_DAQ (defined as in DWG B00000-09-00-680):**

V1 := (VT5\_DAQ + VT6\_DAQ + VT7\_DAQ + VT8\_DAQ + VT9\_DAQ + VT10\_DAQ); //VOLTS //SJ14+ MC01 + SJ01 + MC03 + SJ02 + MC05.1 + SJ03 + MC05.2+SJ04+MC05.3

V2 := (VT11\_DAQ + VT12\_DAQ + VT13\_DAQ + VT14\_DAQ); //VOLTS //SJ05 + MC04 + SJ06 + MC02

V3 := (VT5\_DAQ + VT6\_DAQ + VT7\_DAQ + VT8\_DAQ); //VOLTS //SJ14 + MC01 + SJ01 + MC03

V4 := (VT9\_DAQ + VT10\_DAQ + VT11\_DAQ + VT12\_DAQ + VT13\_DAQ + VT14\_DAQ); //VOLTS //SJ02 + MC05.1 + SJ03 + MC05.2 + SJ04 + MC05.3 + SJ05 + MC04 + SJ06 + MC02

V5 := (VT15\_DAQ + VT16\_DAQ + VT17\_DAQ + VT18\_DAQ + VT19\_DAQ); //VOLTS//SJ07 + VAC\_BREAK\_B + SJ08 + SJ09 + SJ10

V6 := (VT17\_DAQ + VT18\_DAQ + VT19\_DAQ); //VOLTS //SJ08 + SJ09 + SJ10

V7 := (VT5\_DAQ + VT4\_DAQ + VT3\_DAQ + VT2\_DAQ + VT1\_DAQ); //VOLTS //SJ14 + VAC\_BREAK\_A + SJ13 + SJ12 + SJ11

V8 := (VT3\_DAQ + VT2\_DAQ + VT1\_DAQ); //VOLTS //SJ13 + SJ12 + SJ11

V9 := (VT5\_DAQ + VT4\_DAQ + VT3\_DAQ + VT2\_DAQ); //VOLTS // SJ14 + VAC\_BREAK\_A + SJ13 + SJ12

V10 := (VT15\_DAQ + VT16\_DAQ + VT17\_DAQ + VT18\_DAQ); //VOLTS //SJ07 + VAC\_BREAK\_B + SJ08 + SJ09

V11 := (VT6\_DAQ); //VOLTS // MC01

V12 := (VT14\_DAQ); //VOLTS // MC02 V13 := (VT18\_DAQ); //VOLTS // SJ09

V14 := (VT12\_DAQ); //VOLTS // MC04

V15 := VT20\_DAQ; //VOLTS //Whole magnet VCL (-) To VCL(+)

**//Comparators**

COMP1 := V1 - V2; //VOLTS

COMP2 := V3 - V4; //VOLTS

COMP3 := V5 ; //VOLTS

COMP4 := V6; //VOLTS

COMP5 := V7; //VOLTS

COMP6 := V8; //VOLTS

COMP7 := V9; //VOLTS

COMP8 := V10; //VOLTS

COMP9 := V11- V12; //VOLTS

COMP10 := V13 - V14; //VOLTS