Solenoid – Fast Dump Investigations/ Wiring Suggestions

Date: August 28th, 2018
Time: 14:00 – 14:30
Attendees: Pablo Campero, Brian Eng, Ruben Fair, Probir Ghoshal, Amanda Hoebel, Nicholas Sandoval and Scot Spiegel

1. Results of Solenoid quench analysis presented by Ruben Fair
    - 1.1. On 8/27/2018 Solenoid fast dumped at full current 2416 [A].
    - 1.2. PLC SOE module indicated that "Quench Detector (QD) #2 Sum" signal tripped first at 09:12:01 followed by "QD # 1 Sum" and "PLC Fast Dump" signals.
    - 1.3. Compare hardware quench detector units with PLC readout signals, which are showed in Solenoid Interlock Status EPICS screen.
        - 1.3.1. Both, QD #2 unit (A picture of QD#2 was showed as evidence) and PLC matched showing that the trip was in QD#2 at channel 2, which has only VT1_DAQ connected.
    - 1.4. All Solenoid voltage taps, QDs, signals were plotted in the Analyzer tool and the FastDAQ data showed relevant activity (voltage spikes greater than 50 mV) for: VT15_DAQ, VT19_DAQ, VT2_DAQ, VT18_DAQ, and VT1_DAQ.
        - 1.4.1. VT15-DAQ signal presented the first voltage spike ~1V, and then the rest of the VTs mentioned above came before the Fast Dump switch would open.
        - 1.4.2. MPS fast dump switch opened after 180 [ms] from the voltage spike noticed on VT15_DAQ.
2. Discussed abut PLC SOE timestamp offset
    - 2.1. Brian Eng mentioned that PLC timestamps has an offset of 34 s (delayed with respect to Fast Daq data/cRIO) as consequence of changes in the time request configurations.
    - 2.2. Previously PLC used NTP jlab as master clock, now computer center modified this to use PTP.
        - 2.2.1. TTL PLC cannot handle directly PTP configurations due to hardware limitations, Brian Eng contacted Rockwell support to find solutions, but answers are still waiting.
3. Planned forward activities to test Solenoid quench detector units and control systems.
    - 3.1. Locate Resistor Box connectors for the voltage injection.
    - 3.2. Inject voltage at Resistor Box to check behavior of voltage taps: VT15_DAQ, VT1_DAQ.
    - 3.3. Verify that wiring connection matches with current version of the drawings.
    - 3.4. Check wiring to ensure proper channel assignment with Sol-FastDaq-cRIO.
    - 3.5. Check LabVIEW code matches with the wiring connections and channels assigned.
    - 3.6. Record and analyze FastDAQ data during voltage injection.
    - 3.7. Verify set thresholds on QDs and then check if the QDs were reacting properly when the over voltage event was presented.
    - 3.8. Inject voltage on QD#1-ch3 and QD#2-ch4 to see if QDs trip after thresholds are exceeded.
        - 3.8.1. VT15_DAQ appears as part of the voltage tap combination that is connected in QD#1-ch3 (VT15-VT19) and QD#2-ch4 (VT15-VT18).