Jefferson Lab

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HALL B PROCEDURE NO.:
B000000400 –P004 Rev -0

TITLE: **Hall B Solenoid Pre-Power-Up Quench Detector Tuning Procedure**

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DATE: Dec/9th/2016
Intended Checker and Approvers:
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2. APP: 2nd Approver (if necessary)
3. APP: 3rd Approver (if necessary)

completed
P Ghoshal
7/14/2020

Complete and Recorded in the Shared drive./Network.

Conl.: Very good, No drift ✓

REV.	ECO#	DESCRIPTION	BY	CHK.	APP.	APP.	DATE
SUMMARY OF CHANGES FROM PREVIOUS REVISION:							

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Hall B Pre-Power-Up Quench Detector Tuning Procedure

Introduction

The Danfysik System 8500 Multi Quench Detector (QD) detects quenches within the Hall B Solenoid superconducting magnet and is considered as part of the hard-wired protection system

Each QD unit works by comparing:

1. The voltage drops across a pair of coils + splice and triggering a fast dump whenever the voltage imbalance is higher than a pre-set threshold and,
2. Measuring voltage across Vapor Cooled Leads in two separate channels compared to a fixed minimum set threshold voltage.

The Solenoid magnet consists of 5 coils connected in series. C1 is identical to C2, C3 is identical to C4 while C5 is reverse wound to produce a 'shield' coil. The Solenoid magnet therefore has three sets of differing inductance. The quench detection voltage threshold must therefore be set based on the voltage induced during a ramp up to field at the fastest-envisaged ramp rate. During steady state operating conditions, there will be no voltage imbalance between the individual coils as the resistive voltage components (i.e. across splices) will be low."

The C1/C3 and C2/C4 inductance ratios are virtually identical. Therefore, comparing C1+C3 with C2+C4 should yield an inductive voltage (during ramping) that is close to zero. However, in order to provide a measure of redundancy, C5 has been included in the voltage comparison and this will be discussed later within this document. It should be noted that the final voltage thresholds selected will depend on the ambient noise level within the hall and measurement system.

The measured inductances at room temperature have been measured and are available as an Excel file stored on a shared server as follows:

M:\hallb_eng\CLAS12\Magnets\Solenoid\Solenoid test in HALL B\ Hall Solenoid Inductance_expected voltage.xlsx

M:\hallb_eng\CLAS12\Magnets\Solenoid\Solenoid test in HALL B\Hall Solenoid Voltage Tap Wiring Checkouts _Low current measurement.xlsx

Please refer to the wiring diagram (Protection) *DRG#B00000-09-00-0680.*

Please refer the document that defines the hardwired QD limits in order to set up the QD limits. *This is available at the following location for reference:*
M:\hallb_eng\CLAS12\Magnets\Solenoid\Controls and Wiring\ Hall B Solenoid Quench Detector Channel assignment and Voltage Limits for Hardwired QD and Software_November 30th 2016_V1.xlsx

Channel Assignments

- The total calculated Magnet inductance is ~6 H.
- The QD system has EIGHT independent channels.
- The channel #1 and #2 are used to compare the following coils and also include any splices between coils:
    - C1 | C3 | C5 with C4 | C2

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- C1+C3 with C5+C4+C2

- Channels #3 to #8 are independent single channel that covers the splices/bus lead and vapor cooled leads (VCL) which are individually compared to the pre-set quench voltage detection threshold value. The details and limits are defined in the document referenced above (e.g. Channel #1 have 60 mV and Channel #4 have 100 mV). *This is references that are based on estimates. The values might change based on the final assembly and noise in the measurement system.*

Tuning Procedure

1. The initial quench voltage detection threshold will be pre-set to 50 mV (determined at maximum ramp rate to be determined based on the shield coil C5 inductance).
2. In other words, we won't use the balance pot and will include the offset into the threshold. This allows us to use a threshold which is not ramp-rate dependent. Lower ramp rates will have less sensitivity to a simultaneous, full-magnet quench.
3. Each channel has to be adjusted for ZERO balance and then tuned to set the gain to achieve a threshold equivalent to 1.28 V max (trip set by Manufacturer and internal to the circuit board) to account for any imbalance of the channel pair (this should normally be ZERO or in practice may reflect the inherent noise level within the experimental hall itself). The pairs of coils that are being compared are defined by drawing *DRG#B00000-09-00-0680*. The procedure below describes how to perform this adjustment for a given channel. This procedure is then repeated for all the channels since all the coils.
4. **Note the adjustments per channel**: balance, gain and offset are set to have a trip at 1.28V across the amplified comparator.
    a. The balance adjustment accounts for the imbalance between compared coils.
    b. The gain adjustment sets the trip sensitivity.
    c. The offset adjustment ensures that the channel behaves symmetrically during ramp up vs. ramp down. Also note that the offset potentiometer may need to be adjusted to null out induced voltages (not envisaged for the SOLENOID magnet) from the magnet power supply.
5. Use *DRG#B00000-09-00-0680* to check that that you are clear which channel has been assigned to each coil.
6. Calculate the maximum coil voltages for the channel at the highest ramp rate based on calculated inductances (See EXCEL file above). Note that the actual inductances will be re-measured during the commissioning of the solenoid so this procedure may need to be repeated if the difference between the calculated and measured inductances is too large.
7. Turn ON all the QD units.
8. Zero out the channel offset by measuring the voltage at the rear test points and adjusting the rear offset potentiometer until the measured voltage is zero.
9. Using two DC power supplies apply voltage to the high and low channels across the QD unit on the front panel connectors according to the expected maximum voltages during ramp up.

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10. Measure the voltage on the front-panel leads and input to the QD (orange connector) and measure the imbalance through the BNC connector on the front of the QD (numbered 1-8). With injection of 60 or 100 mV across the paired channel (set both +100 mV) the BNC output should ideally read ZERO). *The channels measuring only one input (e.g. bus bars and VCL) with a set 100mV to start with and tune as required based on the noise and expected voltage drop with margin to avoid any spurious trigger of QD.*
11. If the read out is not ZERO, adjust the front-panel balance potentiometer until the voltage drop is zero. At this point the channel is adjusted for the unequal inductances of the coils (if any).
12. Also confirm this adjusted setting by applying a range of other voltages for example 50 mV and 500 mV (to characterize any drift or noise) as reference points only.
13. From this point onwards, the balance potentiometer should not need to be adjusted again unless the measured inductance ratio differs significantly from the calculated values.
14. Increase the voltage on one of the power supplies injecting into the upper channel on the front panel, to the point where you want the channel to trip (e.g. at the 100 mV level). Adjust the front-panel gain potentiometer so that the channel just trips at this offset (voltage measured on the BNC on the front of the QD unit should be 1.28 V).
15. Restore the voltage to the first channel and offset the second channel by the same amount. The QD should trip or be very close to tripping.
16. Now restore and reverse the polarity of both voltages to simulate ramping in the other direction (e.g. ramp down instead of up). Check if both channels trip at the same voltages. If not, adjust the back-panel offset potentiometer to split the difference.
17. Repeat steps 4-16 until the channel trips at the required offsets and trips symmetrically for positive and negative voltages.
18. Repeat the procedure for all the other channels.

Record all the ultimate trip voltages on the Excel spread sheet stored on the shared server at the following location:

M:\hallb_eng\CLAS12\Magnets\Solenoid\Solenoid test in HALL B

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