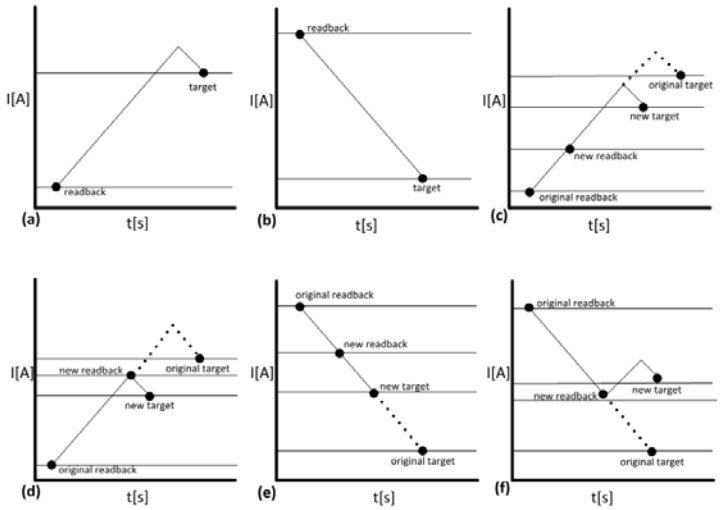
HALL C PLC TASKS REPORT (10/25/2018 – 10/31/2018)

- Fast I/O ADC modules for PLC (model: 1756-IF4FXOF2F/B) researched for potential use in voltage tap data logging for SHMS and HMS PLC systems.
  - Module's four inputs are -10 – +10 V with 14-bit resolution.
    - 1756- IF16/B ADC modules currently in use have eight channels.
  - Module also has two 0 – 20 mA output channels with 13-bit resolution.
  - Maximum recommended data transfer rate uses Requested Packet Interval of 6 ms and a Real-time Sample rate of 300 µs.
    - Data will be logged at ~160 Hz.
- Additional debugging and error handling for PLC communication loss added to SBC's NMR code.
- In Current Loop Regulation Program, ability to hold power supply current if operator turns off current-loop added and is being debugged.
  - Program executes code in the wrong order, causing buttons to require pressing twice to register.
  - Attempted debugging by reordering code on function block diagram, adding additional sheets to function block diagram to force a sequence of execution, and adding a timer between components.
- MPS ramp diagrams created showing the six ramp behaviors tested during development of the Current Loop Regulation Program.
  - **(a)** – ramp behavior if target current is greater than MPS's original readback current when MPS is not ramping.
  - **(b)** – ramp behavior if target current is less than MPS's original readback current when MPS is not ramping.
  - **(c)** – ramp behavior if user inputs a new target current while the MPS is ramping up that is less than the original target current but greater than the MPS's latest current readback.
  - **(d)** – ramp behavior if user inputs a new target current while the MPS is ramping up that is less than both the original target current and the MPS's latest current readback.
  - **(e)** – ramp behavior if user inputs a new target current while the MPS is ramping down that is greater than the previous target current but less than the MPS's latest current readback.
  - **(f)** – ramp behavior if user inputs a new target current while the MPS is ramping down that is greater than both the previous target current and the MPS's latest current readback.



Six diagrams showing the ramp behavior tested in the Current Loop Regulation Program.