The essential part of the Statement of Work for “Design, First Engineering Test Articles, and Sensor QA Validation of HRPPDs (High-Rate Picosecond Photodetectors) Towards a Final EIC Sensor”

The presently anticipated EIC ePIC detector configuration suggests two subsystems to potentially be equipped with HRPPDs: the Backward Ring Imaging Cherenkov (RICH) detector and possibly the high-performance DIRC detector (hpDIRC), to have a total tile count of 68 and 72, respectively. In the following this configuration is labeled as a “final EIC tiles”.

This Statement of Work addresses the required HRPPD sensor modification to be made to the “present design” resulting in the specifications of the “first five EIC tiles” (see the appendix). These first five HRPPD tiles are to be produced following these specifications, and the evaluation process. It is assumed that DC-coupled HRPPDs with internally pixelated anode base plates will be produced, followed by a preliminary evaluation.

The requirements for the “first five EIC tiles” and “final EIC tiles” can be somewhat different, with two basic considerations in mind: (1) all critically important HRPPD modifications should be implemented during the first (re-design) phase and implemented in the production of the first five tiles, (2) incremental changes / improvements between the “first five” and “final” tiles are possible. The full list of requirements is given in the appendix.

Size, active area, material budget

From the mechanical point of view, HRPPDs consist of a pair of Micro-Channel Plates, placed inside of the vacuum volume provided by a ceramic base plate and side walls, and a thick UV Grade Fused Silica window. The existing HRPPD geometry will be modified substantially, without changing the lateral sensor dimensions, in order to (1) increase geometric efficiency, (2) minimize material budget, (3) improve mechanical integration, (4) improve light collection efficiency of the sensor edge area.

Side wall thicknesses will be minimized up to the limits dictated by the vacuum tightness requirements of the window seal. Window and anode base plate thicknesses will be minimized within the limits driven by the tile structural stability under external atmospheric pressure. “Final EIC tiles” will have the photocathode high voltage connection on the rear surface rather than the side wall not extending the tile footprint. HRPPD edges will be cut at 45^0 leaving at least a 5 mm x 5 mm square area at the boundary of four neighboring tiles, thus allow fixing them on a support plate without introducing any substantial lateral gaps during the installation. UV Grade Fused Silica window edges will be optionally tapered and made reflective in order to improve light collection efficiency for Cherenkov photons produced by relativistic charged particles crossing the windows outside of the nominal active area.

MCP configuration

A standard MCP-PMT layout with a pair of 600 μm thick Micro-Channel Plates in a so-called chevron configuration, with 10 μm diameter pores will be used to achieve sufficient gain and timing resolution in the environment of the ePIC solenoid magnetic field. Contrary to the existing HRPPDs, a configuration is foreseen with a non-zero distance between MCP#1 and MCP#2 with separate high voltage tabs to the two MCPs, in order to provide higher gain and more operating flexibility to compensate for the gain loss in a strong magnetic field by an increase in bias voltage.

MCP resistivity requirements for the “final order” will be defined based on the evaluation of the ”first five” tiles, as a compromise between minimizing pore recovery time (suggesting smaller resistivity values) and maintaining the current drawn by a power supply within a ~1mA limit (suggesting larger values).

Internal HV connections

The spring loaded contact interface design inside of the vacuum volume will be revisited regarding its reliability and potential redesign approved by a qualified EIC engineer before the production of the “first five tiles” starts.

External connectivity

Potential existing signal connectivity issues need to be resolved before the production of the “first five tiles” starts, to match the choice of the selected high channel density low power dissipation readout ASIC chips (EICROC). This connectivity allows to mount ASIC readout board(s) directly to the HRPPD rear surface, minimizing the overall sensor assembly volume and simplifying integration in the experiment.

The existing legacy Kyocera design of the HRPPD anode base plates with a uniform 32x32 pad pixellation of the outer surface does not provide convenient means for signal interconnect in a compact configuration with EICROC ASICs, and as such cannot be considered an ideal solution for EIC. The expectation is that the ongoing R&D (independent of this Statement of Work) with a Polish ceramic manufacturer Techtra will result in a better design, which may provide this functionality, and such HRPPD base plates may later be built by Techtra, Kyocera or another PCB shop with the required capability for the final EIC design needs.

Two viable connectivity options will be considered during the first (design modification) phase:

- Screen printing using a conductive epoxy
- High density compression interposers

A custom design of the anode base plate stack with the internal signal traces will be provided by EIC.

High voltage pads on the rear side of the sensors will be replaced by nail head pins of appropriate form-factor, or similar type of interface to simplify the integration.

Electrical safety

The HRPPD design assumes usage of a conductive indium alloy seal between the UV Grade Fused Silica window and the ceramic side wall assembly. This sealing layer is conductive, electrically connected to the photocathode, which is typically operated at 2.0 - 2.5 kV, and it is exposed in the current design.

A way to either electrically isolate this seal using a high dielectric epoxy type material or find a practical way to embed each HRPPD sensor in a thin insulating shell needs to be identified and approved by the authorized EIC personnel before the production of the ”first five tiles” can start.

Active area pixellation

The “first five tiles” will be produced using the presently adopted internal pixellation of the active area of 32x32 square pads.

Performance

HRPPD performance requirements are formulated in terms of the QE peak value, its uniformity across the active area, collection efficiency (CE), achievable gain and gain uniformity, dark count rates (DCR) and transit time spread (TTS) and are specified in the appendix.

Magnetic field tolerance

It should be demonstrated via direct measurements that HRPPD tiles can be operated in the magnetic fields with a strength and orientation matching the locations where sensors will be installed in the EIC detector, for both Backward RICH and hpDIRC cases. Respective input data will be provided by EIC.

"Can be operated" means that the gain can be restored by HV tuning to a level of at least ~10^6.

Production reproducibility

Key performance parameters such as a peak QE, collection efficiency, MCP resistivity at a gain of $5*10^6$, high voltage settings required to achieve this gain at the PC voltage of 100 V, dark count rates, single photon TTS should be reasonably similar across the "first five tiles". The exact bracket for each of these parameters should be defined before the "first five tiles" production starts.

Scope and Deliverables

Incom is to perform the required sensor modifications towards the "first five tiles" specifications, and once successfully achieved, subsequently manufacture five such sensors to allow a sensor QA evaluation process including beam tests.

Appendix

	Present design	First five EIC tiles	Final EIC tiles	Comments
Size, active area, material budget				
Sensor size	~120 mm	~120 mm	120 mm$^{+0\mu m}$	Should stay the same, but meet the increased active area requirement, see below
Active area size	100 mm	104 mm	108 mm	Geometric efficiency optimization; final goal: achieve >80% *fully efficient* active area fraction
UV Grade Fused Silica window thickness	5.0 mm	5.0 mm	4.0 - 5.0 mm	As requested based on Monte Carlo studies
Anode base plate thickness	3.3 mm	3.0 - 3.3 mm	3.0 mm	Minimized to the extent technologically possible
Transfer gaps	no specs	1.0 - 2.0 mm	1.0 - 1.5 mm	Minimized to the extent possible
Side wall width	>4 mm	>4 mm	~3 mm	Optimized for 80% active area requirement
Window tapering	straight	straight	with edge facets	If requested based on Monte Carlo studies
Window edge coating	none	none	reflective	If required by the detector design
Window to Lower Tile Assembly to Anode Alignment	no specs	no specs	< 200 μm	Assume placing tiles in the ~121mm size pockets
MCP configuration				
MCP stack (chevron)	no gap	with a gap	with a gap	Higher gain, more flexible operating voltage choice
MCP pore size	10 μm	10 μm	10 μm	
MCP pore pitch	13 μm	13 μm	13 μm	
MCP thickness	600 μm	600 μm	600 μm	
MCP pore bias angle	13^0	13^0	optionally considered up to 30^0	In case further optimization for a particular magnetic field configuration is required
Resistivity	no specs	no specs	Narrow range to be specified	Given at a gain of $5*10^6$; minimization of a single pore recovery time is a consideration
Internal HV connections				
Spring loaded interface between anode base plate and MCPs	no specs	new robust interface	new robust interface	Design to pass inspection by an authorized EIC electrical engineer
External connectivity				
Anode base plate design	uniform outer pixellation	matching the selected readout PCB	matching the selected ASIC PCB interface	A configurable multi-layer Low Temperature Co-fired Ceramic solution matching the PCB design
ASIC PCB interface	none	optimal out of options (1) … (2)	optimal out of options	Identify and implement the best option out of: (1) high

			(1) … (2)	density compression interconnect, (2) conductive epoxy screen printing
Ground and MCP HV connection	rear side pads	rear side pins or a similar solution	rear side pins or a similar solution	Matching 24 AWG 1.27 O.D. Teflon isolated wire interface
Photocathode HV connection	side wall spot	side wall spot	rear side pin	Same as the MCP HV pins
Electrical safety				
Indium seal electrical isolation	none	none	isolated	Design to pass EIC safety inspection
Active area pixellation	32x32	32x32	on demand, up to 2.5-3.0 mm pad size	Develop capability to implement application-specific pixellation in case EIC RICH and DIRC detectors require different granularity of the anode plane
Environmental & lifetime specs				
Indium alloy melting point	72^0 C	72^0 C	$>100^0$ C	QA thermocycling procedure to be worked out by EIC personnel
QE and gain loss at the extracted charge of 10 C/cm^2	no specs	<10% relative to the initial value	<10% relative to the initial value	Procedure used at UT Arlington to be verified as a reliable non-invasive technique
Performance				
Gain at the photocathode (PC) voltage of 100 V or higher (as required for a high timing resolution)	no specs	$>5*10^6$	$>5*10^6$	Maximum gain at a stable operation; to be used mainly as an indirect quality indicator, since the actual gain in the experiment will most likely be much less than 10^6
Gain non-uniformity across active area	no specs	<20 % RMS	20% with goal <15% RMS	The uniformity is less critical for DC-coupled sensors with a very limited charge sharing
Single photon transit time spread (TTS)	no specs	<60 ps	< 50 ps	As measured at BNL using a femtosecond laser and a high analog bandwidth scope, or a similar equipment
Dark count rate (DCR)	no specs	<2 kHz/cm^2	<2 kHz/cm^2	Evaluated at the PC voltage of 100 V or higher and a gain of 10^6
Quantum efficiency (QE)	no specs	peak value above 27%, with a goal of 30% average across the five sensors	peak value 28-30% or higher across the produced batch	At 330-370nm, measured as an **average value across** the whole active area, using photocathode current against a calibrated photodetector equivalent
QE non-uniformity across active area	no specs	<10% RMS	<10% RMS	Relative to peak value; less important than a high *average* QE across the whole active area
Collection efficiency (CE)	no specs	>80%	>80%	At a threshold used to evaluate the DCR metric, see above; measurement

				procedure to be worked out in the design phase
(Peak QE)*CE product	no specs	>25%	>25%	An alternative metric, ultimately critical for the experiment, in case individual QE or CE parameters are below the specifications above

Table outlining the detailed specifications for the HRPPDs, in various categories. These were logically separated in the text earlier. The column with "First five EIC tiles" is the subject of this Statement of Work. The column with "Final EIC tiles" is illustrative only to outline what is envisioned as the final HRPPD requirements for the EIC detector.