Jefferson Lab

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HALL B PROCEDURE NO.:
B00000401 –P027 Rev -

TITLE: **Hall B Pre-Power-Up Interlock Checkout Procedure**

BY: Nick Sandoval
DATE: 10 / 03 / 2016

Intended Checker and Approvers:
CHK: P. Ghoshal
1. APP: R. Fair
2. APP: D. Kashy
3. APP: 3rd Approver (if necessary)

REV.	ECO#	DESCRIPTION	BY	CHK.	APP.	APP.	DATE
SUMMARY OF CHANGES FROM PREVIOUS REVISION:							

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Goals – Ensure Torus magnet interlock systems are operational prior to powered-up operation (some need to be checked prior to low-current operation, all need to be complete prior to full-current operation)

1. Perform all interlock checks. Some require the magnet to be full of liquid helium and nitrogen

Administrative Requirements

During and after cooldown, complete the appropriate items in Pre Power Up interlock Checklist below. Upload a copy of the completed checklist to the Torus ELOG
https://logbooks.jlab.org/book/hbtorus

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Checks to be performed prior to injecting current to magnet (low-current operation)

PLC Hardware Interlock

10/04/2016	PC/TL	Test Hardwire interlock PLC Chassis watchdog
	✓	Reset the MPS, Reference DWG B00000-09-00-0153
	✓	Remove Timer Relay TYCO CNT-35-96 from DIN socket, wait 5 seconds
	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicates "PLC Chassis Watchdog"
	✓	Reinstall Timer Relay TYCO CNT-35-96 into DIN socket, wait 30 seconds
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/06/2016	PC/TL	Test Hardwire Interlock Current lead water flow (1.4GPM switch)
	✓	Reset the MPS. Reference DWG B00000-09-00-0160 Rev A
	✓	Verify the current lead flow switch circuit is closed
	✓	Verify that water is flowing through the current leads
	✓	Temporarily jumper across the 1.2 GPM switch, Wire 160330
	✓	Slowly close the current lead water supply valve
	✓	Verify that the fast dump breaker has opened (Took about 30 sec.)
	✓	Verify that the SOE indicate "Current Lead Water Flow"
	✓	Unjumper the wire across the 1.2 GPM switch
	✓	Slowly open the current lead water supply valve
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/06/2016	PC/TC	Test Hardwire Interlock Current lead water flow (1.2GPM switch)
	✓	Reset the MPS. Reference DWG B00000-09-00-0160 Rev A
	✓	Verify the current lead flow switch circuit is closed
	✓	Verify that water is flowing through the current leads
	✓	Temporarily jumper across the 1.4 GPM switch, Wire 160330
	✓	Slowly close the current lead water supply valve
	✓	Verify that the fast dump breaker has opened (Took about 30 sec.)
	✓	Verify that the SOE indicate "Current Lead Water Flow"
	✓	Unjumper the wire across the 1.4 GPM switch
	✓	Slowly open the current lead water supply valve
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/04/2016	PC/TL	Test Hardwire Interlock VT Cable Interlock
	✓	Reset the MPS. Reference DWG B00000-09-00-0186 Rev A
	✓	Verify that the VT interlock is closed by all faults clear on GUI
	✓	Disconnect VT cable 180101_C1 from feedthrough

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	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicate "VT cable interlock"
	✓	Reconnect cable 180101_C1 from feedthrough
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
	✓	Repeat the above steps for cables :180101-180110
	✓	cable 180102
	✓	cable 180103
	✓	cable 180104
	✓	cable180105
	✓	cable 180106
	✓	cable180107
	✓	cable180108
	✓	cable180109
	✓	cable180110
10/05/2016	PC/TL	Test Hardwire Interlock System Cable Interlock
	✓	Reference DWG B00000-09-00-0162 Rev A, B00000-09-00-0169 Rev A, B00000-09-00-0172, B00000-09-00-0178
	✓	Verify that the System cable interlock is closed by all faults clear indicating on GUI
	✓	Disconnect System cable 162109_A at connector LC817E1,E2
	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicate "System Cable Interlock"
	✓	Reconnect System cable 162109_A at connector LC817E1, E2
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
	✓	Repeat the above steps for all system cables:
	✓	cable 162426_A at Connector LC817B3,B4
	✓	cable 162509_A at connector LC817C1,C2
	✓	cable 162526_A at connector LC817C3,C4
	✓	cable 162609_A at connector LC817D1,D2
	✓	cable 162626_A at connector LC817D3,D4
	✓	cable 162709_A at connector LC817H1
	✓	cable 162726_A at connector LC817H4
	✓	cable 169141_A at connector 817E1
	✓	cable 169236_A at connector 817E2
	✓	cable 169341_A at connector 817E3
	✓	cable 172108_A at connector 817U1HB1
	✓	cable 172130_A at connector 817D1HB1
	✓	cable 172209_A at connector 817U4HB1

Also checked LC 817 E3, E4

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✓	cable 17229_A at connector 817D4HB1
✓	cable 178131_A at connector 8122C
✓	cable 178231_A at connector 8102
✓	cable 178331_A at connector 8103
✓	cable 178427_A at connector 8104
✓	cable 178531_A at connector 8124
✓	cable 178631_A at connector 8127
✓	cable 178731_A at connector 8125
✓	cabe 178831_A at connector 8128

QD channel Interlock

10/05/2016	AC/TL	**Test Danfysik QD Sum1**
	✓	Reference B00000-09-00-0180 TORUS Voltage Tap Schematic
	✓	Temporarily disassociate the PLC software interlock tag from controlled ramp down and fast dump
	✓	Test QD Ch 1 by inserting a voltage source at Voltage tap using appropriate taps
	✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
	✓	Record the actual trip threshold 194 mV
	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicate "QD Sum1 "
	✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
	✓	Reverse the voltage source leads and repeat the test
	✓	Record the actual trip threshold (-) 197 mV
	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicate "QD Sum1 "
	✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
	✓	Test QD Ch 2 by inserting a voltage source at voltage tap test panel using the appropriate taps
	✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
	✓	Record the actual trip threshold 196 mV
	✓	Verify that the fast dump breaker has opened
	✓	Verify that the SOE indicate "QD Sum1 "
	✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
	✓	Reverse the voltage source leads and repeat the test
	✓	Record the actual trip threshold (-) 196 mV
	✓	Verify that the fast dump breaker has opened

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✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Test QD Ch 3 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 201 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold (-) 198 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Test QD Ch 4 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 199 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold (-) 203 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS

PC/TL	**Test Danfysik QD Sum2**
✓	Reset the MPS, Refer to B00000-09-00-0180 TORUS Voltage Tap Schematic
✓	Temporarily disassociate the PLC software interlock tag with ramp down and fast dump
✓	Test QD Ch 5 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 197 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold - 217 mV

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✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Test QD Ch 6 by inserting a voltage source at voltage tap test panel using the appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 197 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold (-) 216 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Test QD Ch 7 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 100 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold (-) 94 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Test QD Ch 8 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 97 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold -104 mV
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS

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10/05/2016

PC/TL	Test Danfysik QD Sum3
✓	Reset the MPS, Refer to B00000-09-00-0180 TORUS Voltage Tap Schematic
✓	Temporarily disassociate the PLC software interlock tag with ramp down and fast dump
✓	Test QD Ch 1 by inserting a voltage source at Voltage tap using appropriate taps
✓	Slowly raise the voltage in 5mV increments starting at 50mV until threshold is hit
✓	Record the actual trip threshold 2.275 V
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS
✓	Reverse the voltage source leads and repeat the test
✓	Record the actual trip threshold (-) 2.126 V
✓	Verify that the fast dump breaker has opened
✓	Verify that the SOE indicate "QD Sum1 "
✓	Reduce voltage source to 0mV, clear the interlock/reset MPS

10/04/2016

PC/TL	Test PLC Fast Dump Button(Epic's GUI
✓	Verify all interlocks are clear
✓	on the interlock screen depress the fast dump button
✓	Click yes when the prompt comes up "are you sure you want to do this"
✓	verify that the dump contactor opened
✓	Verify that the SOE indicates "PLC fast dump"
✓	In PLC Expert screen verify that the GUI button was the source for opening the PLC fast dump sum
✓	Reset the MPS, Verify all interlocks are clear

10/04/2016

PC/TL	Test PLC Hard coded current limit
✓	Verify all interlocks are clear
✓	In the PLC expert screen disassociate the MPS current tag from the hard coded current limit
✓	Insert a test tag with a number greater than **3800A**
✓	Verify that the dump contactor opened
✓	Verify that the SOE indicates "PLC fast dump"

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	✓	In PLC Expert screen verify that the hard current was the source for opening the PLC fast dump sum
	✓	Reset the MPS, Verify all interlocks are clear
10/04/2016	AC/TL	Test PLC ramp down failure
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen disassociate the di/dT tag from the ramp down failure routine
	✓	Insert a test tag with a number less than 2.0A/s
	✓	Initiate a "controlled ramp down" by forcing the sum bit true
	✓	Verify that the dump contactor opened
	✓	Verify that the SOE indicates "PLC fast dump"
	✓	In PLC Expert screen verify that the ramp down monitor was the source for opening the PLC fast dump sum
	✓	Reset the MPS, Verify all interlocks are clear

	PC/TL	Test PLC VESDA fire detection
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen force the "VESDA" bit true
	✓	Verify that the dump contactor opened
	✓	Verify that the SOE indicates "PLC fast dump"
	✓	In PLC Expert screen verify that the VESDA bit was the source for opening the PLC fast dump sum
	✓	Reset the MPS, Verify all interlocks are clear

10/06/2016	AC/TL	Test PLC Software quench, 2nd threshold
	✓	Disable the three hardwire QD sums with "flagged" jumpers
	✓	Disable the PLC QD controlled ramp down by temporarily raising the thresholds to 250mV
	✓	Verify that the VT panel is isolated from the magnet checking position of switches
	✓	The below steps will be repeated and recorded for each of the ten comparators:
10/06/2016	PC/TL	Comparator 1
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT8-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump

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	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 126 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 2
	✓	Place voltage source1 on VT9-DAQ and set it at 200mV
	✓	Place voltage source2 on VT12-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 184 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
	PC/TL	Comparator 3
	✓	Place voltage source1 on VT13-DAQ and set it at 200mV
	✓	Place voltage source2 on VT16-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 126 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 4
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT10-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 28 mV
	✓	Remove both sources

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	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 5
	✓	Place voltage source1 on VT9-DAQ and set it at 200mV
	✓	Place voltage source2 on VT14-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 235 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 6
	✓	Place voltage source1 on VT13-DAQ and set it at 200mV
	✓	Place voltage source2 on VT6-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	X	Record the difference of source 1 and source2 Trips continuously on noise in VT6-DAQ
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 7
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT18-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 198 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 8
	✓	Place voltage source1 on VT3-DAQ and set it at 200mV
	✓	Place voltage source2 on VT19-DAQ and set it at 80mV

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	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 200 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 9
	✓	Place voltage source1 on VT2-DAQ and set it at 200mV
	✓	Place voltage source2 on VT20-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the ramp PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 198 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 10
	✓	Place voltage source1 on VT1-DAQ and set it at 200mV
	✓	Place voltage source2 on VT21-DAQ and set it at 80mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the dump contactor opened
	✓	Verify the SOE indicate "PLC Fast dump
	✓	In PLC Expert screen verify that the ramp PLC QD was the source for opening the PLC fast dump sum
	✓	Record the difference of source 1 and source2 198 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
	✓	Enable the PLC QD controlled ramp down by lowering the thresholds to 100mV
	✓	Reinstall the three hardwire QD sums be removing "flagged" jumpers

10/04/2016	PC/TL	Test PLC UPS battery low signal
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen force the "PLC UPS battery Low"

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	✓	Verify that the dump contactor opened
	✓	Verify that the SOE indicates "PLC fast dump"
	✓	In PLC Expert screen verify that the UPS battery Low was the source for opening the PLC fast dump sum
	✓	Reset the MPS, Verify all interlocks are clear

10/06/2016	PC/TL	Test ESR (End Station Refrigerator Fault)	
	✓	Verify all interlocks are clear	
	✓	In the PLC expert screen force the "ESR Fault" bit	
	✓	Verify that the dump contactor opened →	Does not open contactor – PLC code changed to cause Controlled Ramp Down
	✓	In PLC Expert screen verify that the ESR fault was the source for opening the PLC fast dump sum	
	✓	Reset the MPS, Verify all interlocks are clear	

10/04/2016	PC/TL	Axial Support SG Controlled Ramp Down	
	✓	Verify all interlocks are clear	
	✓	In the PLC expert screen associate a temporary tag as the Axial SG with a value higher than the current limit	
	✓	Verify that the MPS ramp down was initiated via comms routine	
	✓	In PLC Expert screen verify that the Axial SG was the source for ramp down sum	
	✓	Remove the temporary test tag and re-associate correct tag	
	✓	Reset the MPS, Verify all interlocks are clear	
10/04/2016	PC/TL	DS Hex Beam SG Controlled Ramp Down	
	✓	Verify all interlocks are clear	
	✓	In the PLC expert screen associate a temporary tag as the DS Hex Beam SG with a value higher than the current limit	
	✓	Verify that the MPS ramp down was initiated via comms routine	
	✓	In PLC Expert screen verify that the DS Hex Beam SG was the source for ramp down sum	
	✓	Remove the temporary test tag and re-associate correct tag	
	✓	Reset the MPS, Verify all interlocks are clear	
10/04/2016	PC/TL	US Hex Beam SG Controlled Ramp Down	
	✓	Verify all interlocks are clear	
	✓	In the PLC expert screen associate a temporary tag as the US Hex Beam SG with a value higher than the current limit	
	✓	Verify that the MPS ramp down was initiated via comms routine	
	✓	In PLC Expert screen verify that the US Hex Beam SG was the source for ramp down sum	
	✓	Remove the temporary test tag and re-associate correct tag	

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	✓	Reset the MPS, Verify all interlocks are clear
10/05/2016	PC/TL	CCM Load Cell Controlled Ramp Down
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen associate a temporary tag as the CCM Load Cell with a value higher than the current limit
	✓	Verify that the MPS ramp down was initiated via comms routine
	✓	In PLC Expert screen verify that the CCM Load Cell was the source for ramp down sum
	✓	Remove the temporary test tag and re-associate correct tag
	✓	Reset the MPS, Verify all interlocks are clear
10/05/2016	PC/TL	Vertical Support Controlled Ramp Down
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen associate a temporary tag as the Vertical Support with a value higher than the current limit
	✓	Verify that the MPS ramp down was initiated via comms routine
	✓	In PLC Expert screen verify that the Vertical Support was the source for ramp down sum
	✓	Remove the temporary test tag and re-associate correct tag
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	Software Quench, 1st threshold Controlled Ramp Down
	✓	Disable the three hardwire QD sums with "flagged" jumpers
	✓	Disable the PLC QD ~~fast ramp down~~ 2nd Threshold by temporarily raising the thresholds to 250mV
	✓	Verify that the VT panel is isolated from the magnet checking position of switches
	✓	The below steps will be repeated and recorded for each of the ten comparators:
10/06/2016	PC/TL	Comparator 1
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT8-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the ~~Fast~~ Controlled Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 123 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 2
	✓	Place voltage source1 on VT9-DAQ and set it at 200mV
	✓	Place voltage source2 on VT12-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip

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	✓	Verify the ~~Fast~~ Controlled Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 128 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 3
	✓	Place voltage source1 on VT13-DAQ and set it at 200mV
	✓	Place voltage source2 on VT16-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 120 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 4
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT10-DAQ and set it at 120mV Trips continuously on noise in VT10-DAQ
	X	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the ~~Fast~~ Controlled Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	X	Record the difference of source 1 and source2
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 5
	✓	Place voltage source1 on VT9-DAQ and set it at 200mV
	✓	Place voltage source2 on VT14-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the ~~Fast~~ Controlled Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 6

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	✓	Place voltage source1 on VT13-DAQ and set it at 200mV
	✓	Place voltage source2 on VT6-DAQ and set it at 120mV
	X	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	X	Record the difference of source 1 and source2
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 7
	✓	Place voltage source1 on VT5-DAQ and set it at 200mV
	✓	Place voltage source2 on VT18-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	~~Verify the dump contactor opened~~ Controller
	✓	Verify the ~~Fast~~ Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 149 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 8
	✓	Place voltage source1 on VT3-DAQ and set it at 200mV
	✓	Place voltage source2 on VT19-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
		~~Verify the dump contactor opened~~ Controller
	✓	Verify the ~~Fast~~ Ramp Down was initiated
	✓	In PLC Expert screen verify that the PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 145 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 9
	✓	Place voltage source1 on VT2-DAQ and set it at 200mV
	✓	Place voltage source2 on VT20-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
		~~Verify the dump contactor opened~~ Controller
	✓	Verify the ~~Fast~~ Ramp Down was initiated

* Trips continuously on noise in VT6-DAQ

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	✓	In PLC Expert screen verify that the ramp PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 149 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
10/07/2016	PC/TL	Comparator 10
	✓	Place voltage source1 on VT1-DAQ and set it at 200mV
	✓	Place voltage source2 on VT21-DAQ and set it at 120mV
	✓	Slowly decrease the voltage on source2 by 5mV increments until you get a trip
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the ramp PLC QD was the source for initiating the fast ramp down
	✓	Record the difference of source 1 and source2 148 mV
	✓	Remove both sources
	✓	Clear the interlock fault on the GUI or "PLC Expert Screen"
	✓	Enable the PLC QD controlled ramp down by lowering the thresholds to 100mV
	✓	Reinstall the three hardwire QD sums be removing "flagged" jumpers
10/05/2016	PC/TL	Vacuum Interlock Controlled Ramp Down
	✓	Verify all interlocks are clear
	✓	In the PLC expert screen force associate a temporary test tag to the vacuum interlock and raise the value above threshold
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the vacuum was the source for initiating the PLC fast ramp down
	✓	Remove test tag and re-associate the correct tag
	✓	Reset the MPS, Verify all interlocks are clear
10/05/2016	PC/TL	EPIC's WatchDog Controlled Ramp Down
	✓	Verify all interlocks are clear
	✓	In the EPICS expert screen force stop on the heartbeat
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the EPIC's Watchdog was the source for initiating the PLC fast ramp down
	✓	Re-enable EPIC's heartbeat
	✓	Reset the MPS, Verify all interlocks are clear

Cryogenics Control

10/06/2016	PC/TL	Helium Pressure Controlled Ramp Down (requires at least 2.0ATM of helium)

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	✓	Verify all interlocks are clear
	✓	Lower the interlock threshold to 1.9ATM
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the Helium Pressure interlock was the source for initiating the fast ramp down
	✓	Raise the helium pressure interlock back to 2.5ATM → reset to 3.6, as before test
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	Nitrogen Pressure Controlled Ramp Down (requires at least 1.0ATM of nitrogen)
	✓	Verify all interlocks are clear
	✓	Lower the interlock threshold to 0.5ATM
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the Nitrogen Pressure interlock was the source for initiating the fast ramp down
	✓	Raise the nitrogen pressure interlock back to 0.9ATM
	✓	Reset the MPS, Verify all interlocks are clear
	~~PC~~	~~Nitrogen Pressure Controlled Ramp Down (requires at least 1.0ATM of nitrogen)~~
		~~Verify all interlocks are clear~~
		~~Lower the interlock threshold to 0.5ATM~~ * repeat of above
		~~Verify the Fast Ramp Down was initiated~~
		~~In PLC Expert screen verify that the Nitrogen Pressure interlock was the source for initiating the fast ramp down~~
		~~Raise the nitrogen pressure interlock back to 0.9ATM~~
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	Lhe Liquid Level Controlled Ramp Down Lower(requires at least 20% helium)
	✓	Verify all interlocks are clear
	✓	Raise the interlock threshold to 22%
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
	✓	Return the Lhe LL interlock back to 20%
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	Lhe Liquid Level Controlled Ramp Down Upper (requires at least 20% helium)
	✓	Verify all interlocks are clear
	✓	Lower the interlock threshold to 18%
	✓	Verify the Fast Ramp Down was initiated

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	✓	In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
	✓	Raise the Lhe LL interlock back to 90%
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	LN2 Liquid Level Controlled Ramp Down Lower (requires at least 20% helium)
	✓	Verify all interlocks are clear
	✓	Raise the interlock threshold to 22%
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
	✓	Return the Lhe LL interlock back to 20%
	✓	Reset the MPS, Verify all interlocks are clear
10/06/2016	PC/TL	LN2 Liquid Level Controlled Ramp Down Upper(requires at least 20% helium)
	✓	Verify all interlocks are clear
	✓	Lower the interlock threshold to 18%
	✓	Verify the Fast Ramp Down was initiated
	✓	In PLC Expert screen verify that the Lhe LL interlock was the source for initiating the fast ramp down
	✓	Return the Lhe LL interlock back to 90%
	✓	Reset the MPS, Verify all interlocks are clear
10/07/2016	PC/TL	Verify interlocks to prevent over-current
	✓	Verify code does not allow user to enter current higher than planned in procedure
	✓	Verify code triggers a controlled discharge if current limit is exceeded
	✓	Verify hardware limit in power supply is set to maximum current expected during procedure

* EPICS would not allow any current set point to be entered.

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Checks to be performed prior to full-current operation

Depending on time elapsed between low-current and full-current operations, repeat some of the pre-checks that are deemed necessary to resume operations. In addition, the following checks are to be completed prior to full-current operation (or could happen in parallel to low-current operations).

☐	Verify that interlocks for magnet mechanical monitoring are finalized (spreadsheet) and operational
☐	Verify interlocks for support forces
☐	Verify interlocks for hex-beam forces
☐	Verify interlocks for hub forces
☐	Verify interlocks for combined load scenarios

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Note:
VX is the derived parameters and VTXX_DAQ (defined as in DRG B00000-09-00-180):

```
V1 := (VT5_DAQ  + VT6_DAQ  + VT7_DAQ);//VOLTS//S3 + Coil A + S10

V2 := (VT7_DAQ  + VT8_DAQ  + VT9_DAQ);//VOLTS//S4 + Coil B + S3

V3 := (VT9_DAQ  + VT10_DAQ + VT11_DAQ);//VOLTS//S4 + Coil C + S5

V4 := (VT11_DAQ + VT12_DAQ + VT13_DAQ);//VOLTS//S6 + Coil D + S5

V5 := (VT13_DAQ + VT14_DAQ + VT15_DAQ);//VOLTS//S1 + Coil E + S6

V6 := (VT15_DAQ + VT16_DAQ + VT17_DAQ);//VOLTS//S1 + Coil F + (S7 + S2)//Lead
In resistive voltages

V7  := (VT5_DAQ  + VT4_DAQ  + VT3_DAQ);//VOLTS//S10 + Vac_break_in +
Lead_Ext_In

V8  := (VT3_DAQ);//VOLTS//S9 + Lead_Ext_In

V9  := (VT2_DAQ);//VOLTS//Lead Ext solder joint @ vcl cold end IN

V10 := (VT1_DAQ);//VOLTS//VCL In

V16 := (VT1_DAQ + VT2_DAQ + VT3_DAQ + VT4_DAQ + VT5_DAQ);//VOLTS// Resistive
section IN

//whole magnet V11 := VT22_DAQ;//VOLTS//Whole magnet RT lead to lead

//V18 := VTXX_DAQ/1000000;//VOLT//Whole magnet 4.2K lead to lead
VTXX_DAQ: VT2_DAQ + VT3_DAQ + VT4_DAQ + VT5_DAQ + VT6_DAQ + VT7_DAQ + VT8_DAQ
+ VT9_DAQ + VT10_DAQ + VT11_DAQ + VT12_DAQ + VT13_DAQ + VT14_DAQ + VT15_DAQ +
VT16_DAQ + VT17_DAQ + VT18_DAQ + VT19_DAQ + VT20_DAQ

//Lead Out resistive voltages
V12 := (VT21_DAQ);//VOLTS//VCL Out
```