CLAS12 Silicon Vertex Tracker

Technical Design Report

Version 1.0

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Contents

1 Physics Requirements for CLAS12 Tracking

The CLAS detector in Hall B is being upgraded to take advantage of the increase of the CEBAF beam energy from 6 to 12 GeV, thus the new name, CLAS12. There are several broad areas of physics enquiry that drive these changes: spectroscopic studies of excited baryons, investigations of the influence of nuclear matter on propagating quarks, studies of polarized and unpolarized quark distributions, and a comprehensive measurement of generalized parton distributions (GPDs). Many of the reactions of interest are electroproduction of exclusive and semi-inclusive final states. The cross sections for these processes are small, necessitating high-luminosity experiments. A variety of simulated experiments rely on luminosities of 10^{35} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ to achieve the desired statistical accuracy in runs of a few months duration. The new kinematic range to be explored is characterized not only by smaller cross sections, but also by more outgoing particles per event, with those particles being emitted with higher values of momentum and at smaller laboratory angles. These basic physics criteria drive the design.

The deep exclusive reactions, in which an electron scattering at moderate to high values of Q^2 results in a meson-baryon final state, provide the most stringent requirements for the CLAS12 tracking system. A final state of a few high-momentum, forward-going particles (the electron as well as one or more mesons), combined with a moderate-momentum baryon emitted at large angles, is the typical event type that determines the specifications of the tracking system.

The higher momentum and more forward angles of most hadrons leads us to split the design into a "forward" detector, which covers lab angles between 5° and 40°, and a "central" detector for hadrons with angles greater than 35°. The higher luminosity goal necessitates the use of a solenoidal magnet to shield the detector from Møller electrons. To reduce interactions between this solenoidal field and the main CLAS12 toroidal field, and to facilitate construction and installation of new detector elements, the torus has been re-designed. It is more compact than the present CLAS torus, while providing equivalent bending power. This smaller torus design provides several advantages in the overall detector design: it decouples the design of the central solenoid and detector from that of the torus and forward tracking system, and it makes detector installation and removal easier.

In broad strokes, the detector must provide tracking for laboratory angles as small as 5°

and as large as 125° in order to cover as much of the hadronic center-of-mass region as possible. We require very good momentum and angular resolution for the scattered electron in order to determine the virtual photon flux factor, Γ_v, to an accuracy of a few percent. Because the average particle momenta will be higher, the resolution of the tracking system must be better than the current CLAS values; the goal for the fractional momentum resolution is 0.5% to 1% at a track momentum of 5 GeV. Angular resolutions of about 1 mrad are required for the electron in order to know the virtual photon flux factor, and hence, the cross section, to a few percent. Finally, good vertex resolution will allow detection of secondary decay vertices and serve as a good marker for strangeness production.

Because only about 20% of the total charged particle momenta is carried by tracks in the central region, the fractional momentum resolution requirement for the central tracking system at a momentum of 1 GeV is 5% in order to match the absolute momentum resolution of the forward tracking system. This momentum resolution of about 50 MeV is necessary in order to positively identify a missing pion in these exclusive reactions. Similarly, to keep our knowledge of the individual vector components of the momentum at the 25 MeV level, the central trackers angular resolution should be of the order of 1.5°. Our present design has an expected performance about a factor of two better than these simple limits.

A tracking system capable of achieving these standards was described in the PCDR [1] and quantitatively parameterized in a "fast" Monte Carlo program [2]. A number of CLAS collaborators used the model of the detector as described in FASTMC in proposals presented at JLab PAC30 and PAC32 [3, 4].

2 Tracking System Design

As noted above, the CLAS12 detector is divided into a forward and a central detector. Fig 1 shows a perspective view of the CLAS12 detector. A solenoid magnet surrounds the target, followed by a Møller absorber on the beam-line and a high-threshold Čerenkov counter for electron identification. Besides curling background Møller electrons into the absorber, the solenoid provides a nearly constant magnetic field that allows charged particle momentum determination by a set of "central tracking chambers" consisting of 8 layers of silicon strip sensors. This central tracking region covers polar angles from 35° to 125°. Just downstream of the cylindrical central tracker are the "forward vertex chambers": 6 layers of silicon strip cham-

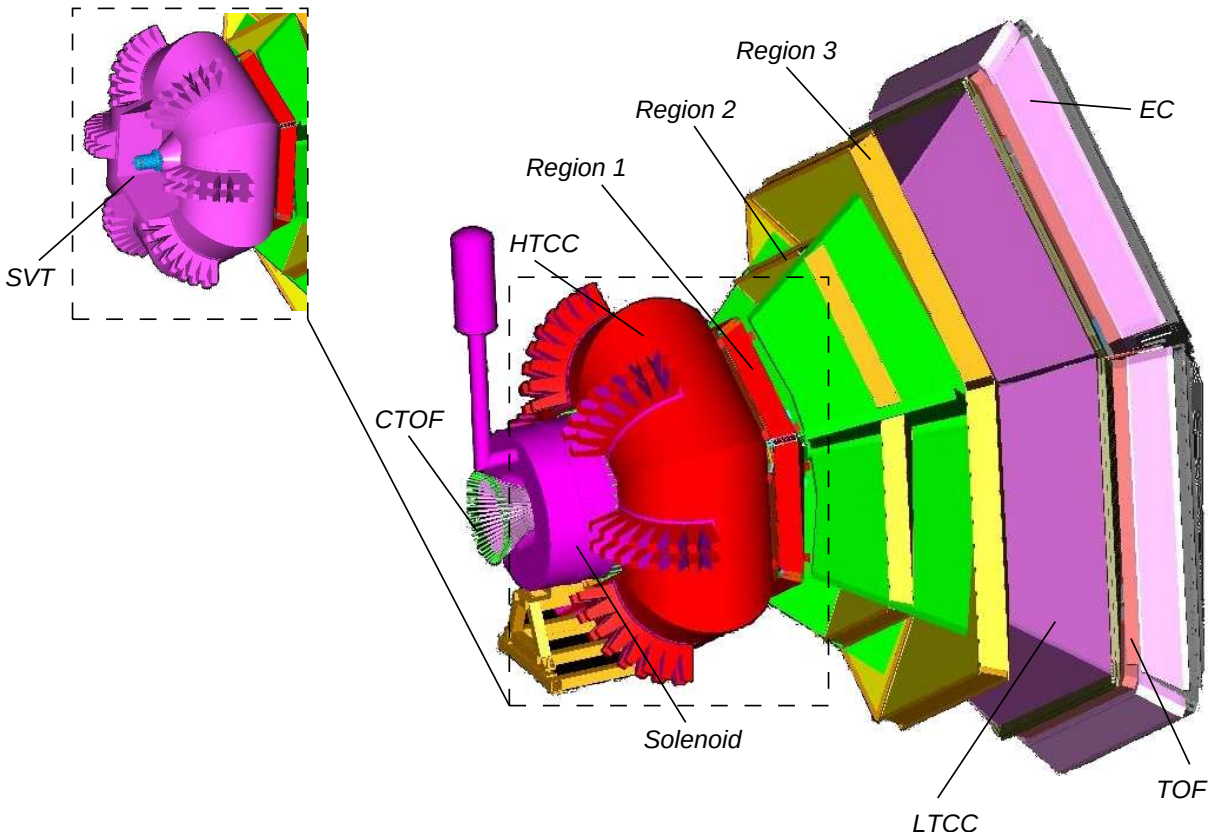

Figure 1: A three-dimensional view of the proposed CLAS12 detector highlighting the various subsystems. The small inset on the left shows the same area highlighted by the dashed box on the right but with the solenoid removed to show the SVT system.

bers. Downstream of the high-threshold Čerenkov counter is the torus magnet that supports three "regions" of "forward drift chambers", designated as Regions 1, 2, and 3. Surrounding and downstream of the torus/drift chamber assembly are the forward time-of-flight counters, a low-threshold Čerenkov counter for hadron identification, and two sets of electromagnetic shower counters. This document describes each of the elements of the CLAS12 tracking system, the central tracker, the forward vertex tracker, and the forward drift chambers.

We have designed the tracking detectors with these external constraints: a solenoid of 5 T central field value and a radius available for tracking detectors of 25 cm, a new torus with a different aspect ratio but with the same number of amp-turns as the present CLAS torus, an expected background rate consistent with a luminosity of 10^{35} cm^{-2}s^{-1}, and a separation between the "forward" and "central" regions defined to be at about 40°; specifically the forward tracking chambers are designed to cover scattering angles between 5° and 40° and the central tracker will cover 35° to 125°. Although the torus cryostat will limit the azimuthal

coverage to about 50% at 5°, our goal is that the inactive portion of the drift chambers not further intrude into the active volume; i.e. the dead areas of the drift chambers (endplates, electronics, etc.) will be located in the "shadow" of the coil as viewed from the target. For Region 2, this is not possible; but we shall try to minimize this dead area. To summarize, we are designing the CLAS12 tracking system with the requirements shown in Table 1.

	Fwd. Tracker	**Central Tracker**
Angular coverage	5° - 40°	35° - 125°
Momentum resolution	$dp/p < 1\%$	$dp/p < 5\%$
θ resolution	1 mrad	1 mrad
θ resolution	1 mrad	5 - 10 mrad
ϕ resolution	1 mrad/$\sin\theta$	5 mrad/$\sin\theta$
Luminosity	10^{35} cm^{-2}s^{-1}	10^{35} cm^{-2}s^{-1}

Table 1: General specifications for CLAS12 tracking.

2.1 Forward Tracking Design

The higher beam energies available to CLAS12 mean that tracks will go more forward and have higher momenta than for the present CLAS experiments. We thus require better resolution from the forward drift chambers. Our design should give better spatial resolution than the present CLAS chambers for several reasons: the use of thicker (30-μm diameter) sense wires will result in a more linear drift velocity, all cells in a superlayer will be identical, easing the calibration, and the simpler mechanical structure should make these chambers easier to survey. The other feature of higher energy and associated smaller cross sections, requires the use of higher intensity beams. The resultant higher backgrounds represent the primary motivation for the central solenoidal magnet and Møller absorber. The higher background can also be mitigated by cells that cover a smaller angular range and have a smaller active time window.

Forward tracks (angles between 5° and 40°) will be momentum-analyzed by passing through the magnetic field of the torus. The magnet provides an integral Bdl of almost 3 T-m at 10°, falling to about 1 T-m at 30° (see Fig. 2).

Such forward tracks will first pass through six layers of the forward silicon vertex tracker

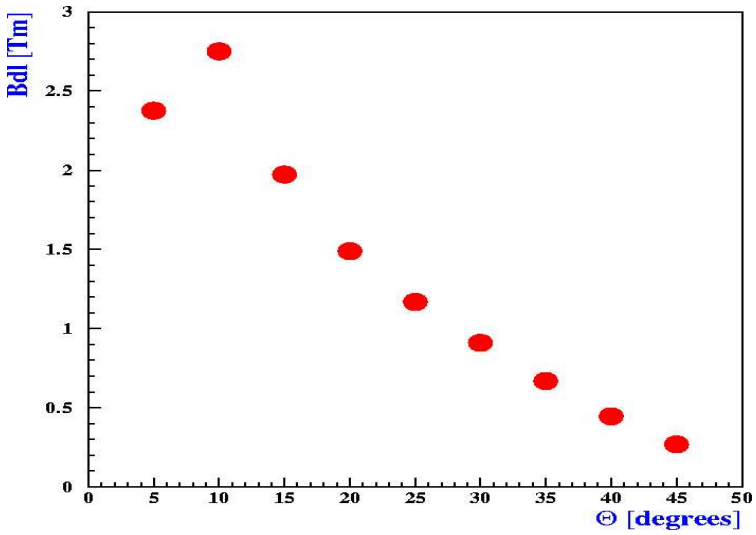

Figure 2: The integral of the B field times path length along rays from the target at various angles.

(FST); a silicon strip tracker with a strip pitch of 150 μm arranged with alternating V-W stereo layers with a stereo angle of $\pm 12°$, located about 27 cm from the target. These tracks will then traverse the high-threshold Čerenkov counter (HTCC) before entering the Region 1 drift chamber at a distance of 2.1 m from the target. The track continues through the magnetic field region and its trajectory is measured in two more drift chambers, denoted Regions 2 and 3, respectively. The Region 2 and 3 chambers are located at 3.3 and 4.5 m from the target, respectively. The FST should localize hits with an estimated accuracy of about 50 μm perpendicular to the strip direction, while the three regions of drift chambers are expected to have spatial resolutions of about 250 μm per layer. The expected momentum resolution from such an assembly is a function of angle, ranging from about 0.3% at 5° to about 1.0% at 30°, and nearly constant as a function of momentum. The angular resolution falls rapidly with increasing momentum, but should be better than 2 mrad at a momentum of 1 GeV. See Section 7 for plots of the results of our simulations.

2.2 Central Tracking Design

The momentum and angular resolution goals for the central tracker are set by the requirement that we be able to positively identify a single missing pion; roughly a 50 MeV momentum resolution is needed, i.e. a fractional momentum resolution of 5% or better at a track momentum of 1 GeV. Our design consists of 8 layers of silicon strips with alternating plus and minus stereo angle strips. Each detector plane is formed as a polygonal shell with the silicon strips

running along the z-direction. Each single-sided layer is comprised of 300-μm thick silicon. This detector has good intrinsic resolution in the r-ϕ coordinate due to the small strip pitch (150 μm readout and 75 μm implant pitch). It relies on a small stereo angle to determine the r-z position of tracks.

A solenoidal magnet contains the target, the silicon vertex tracker, the central time-of-flight system (CTOF), and the Møller absorber. Charged particles with emission angles greater than 35° follow helical paths through the 8 layers of the BST, which are arranged into four V-W modules with "V" and "W" referring to strip orientations. The time resolution of the CTOF ($\sim$60 ps) will enable particle identification of the charged tracks, as well as allowing for a very efficient rejection of out-of-time accidentals.

3 Design

3.1 Overview

The Silicon Vertex Tracker (SVT), anticipated to have $\sim$65,000 channels, will consist of a forward silicon tracker (FST) and a barrel silicon tracker (BST). The θ-coverage of the forward part is from 5° to 35° and that of the barrel part is from 35° to 125°. Conceptual design studies started in 2004 [5]. For both the forward and barrel parts, the ϕ coverage is nearly 2π. The SVT will be centered inside the 1800-mm long solenoid, that has an outer and inner diameter of 2040 mm and 780 mm, respectively .

3.2 Configuration

Several configurations of the BST and the FST were studied [6] with the aim to optimize the layout with respect to operability, performance and cost. The BST is designed to have four regions and the FST is designed to have three regions. The BST and FST form two independent detectors (see Fig. 4), providing operational flexibility in that either or both detectors could be used in a given experiment. There are only three FST regions because the FST will be used in conjunction with the three drift chambers in the forward region.

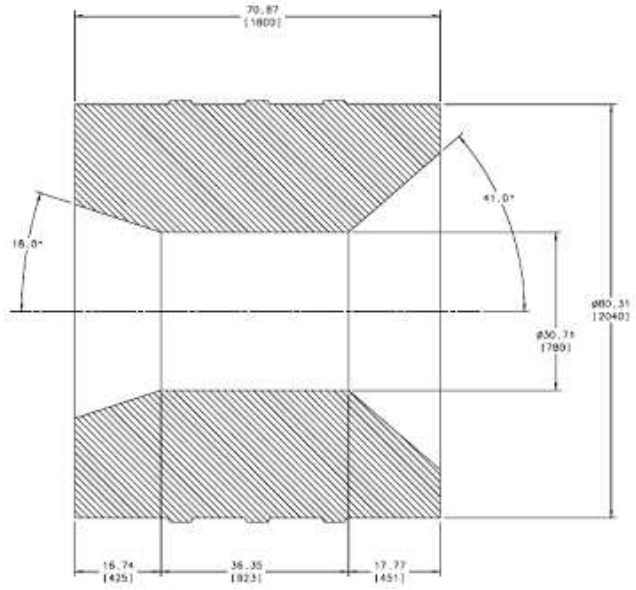

Figure 3: Side view of the solenoid magnet (units in inches – with mm in parentheses).

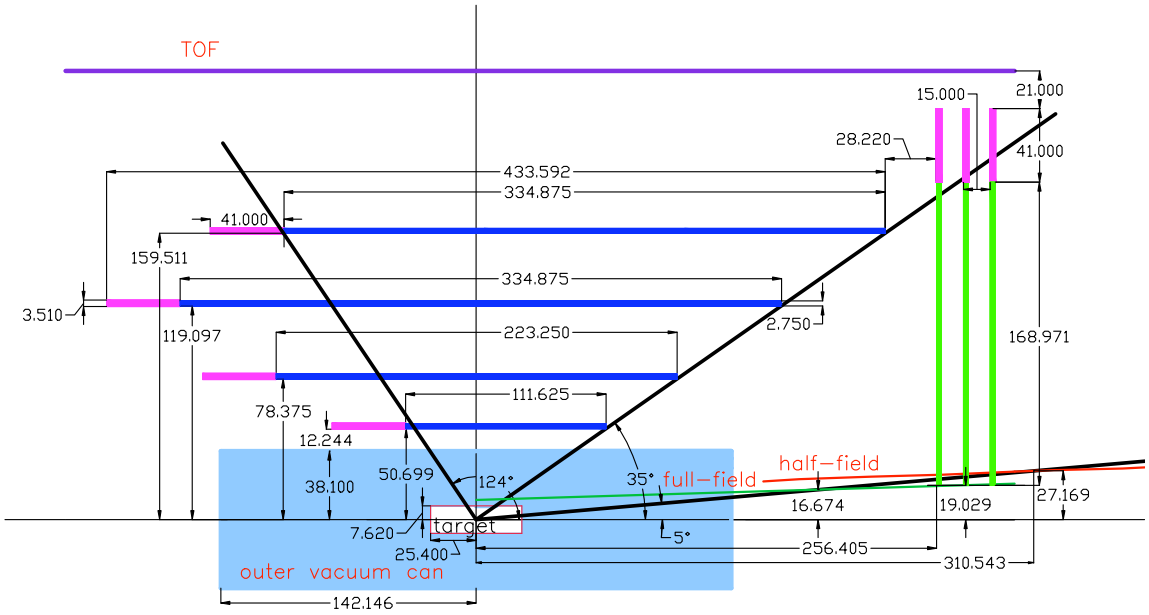

Figure 4: Side view of the SVT showing the layout of the barrel and forward regions (all dimensions in mm).

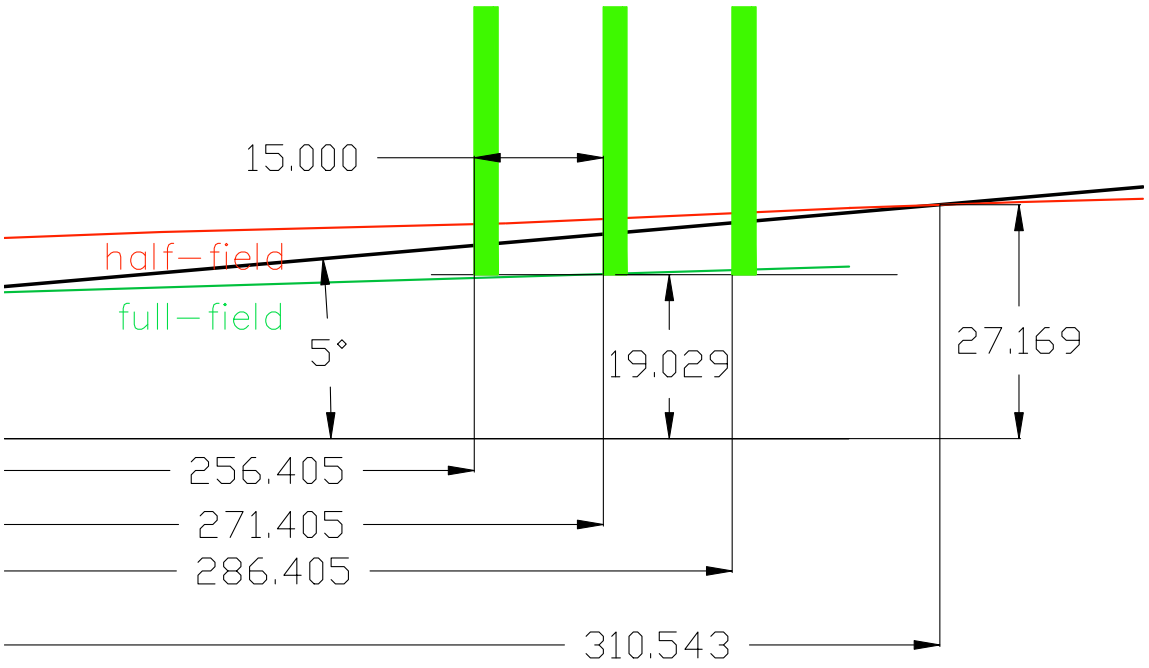

Figure 5: Close up view of the three forward SVT regions near the beam line and the Møller absorber.

3.3 Rate Estimates

Event and background rates were estimated using a GEANT simulation [7, 8]. These studies indicate that the maximum rate, including electromagnetic background for a full-field setting of the solenoid (5 T) is ∼40 MHz in the FST and ∼60 MHz in the BST. In Fig. 4, the green and red curve (full and half-field settings of the solenoid) along the beam axis is the Møller electron envelope, on the surface of which the rate is ∼1 MHz. The rate drops rapidly with increasing scattering angle [8].

To keep Møller electron rates on the FST sensors less than 1 MHz, the first region of the FST is placed at z=256.405 mm (see Figs. 4 and 5), past the intersection of the Møller electron envelope for the full-field setting with the keep-out zone, defined to be a cone with a half opening angle of 5°. The second and third regions of the FST are at z=271.405 mm and z=286.405 mm, respectively.

3.4 Forward Silicon Tracker (FST)

The trapezoidal sensors of the FST are designed to be identical. Such a design requires that the regions be parallel to the beam axis, rather than ride the 5° keep-out cone. In ϕ, each

FST region consists of 15 sectors as shown in Fig. 6.

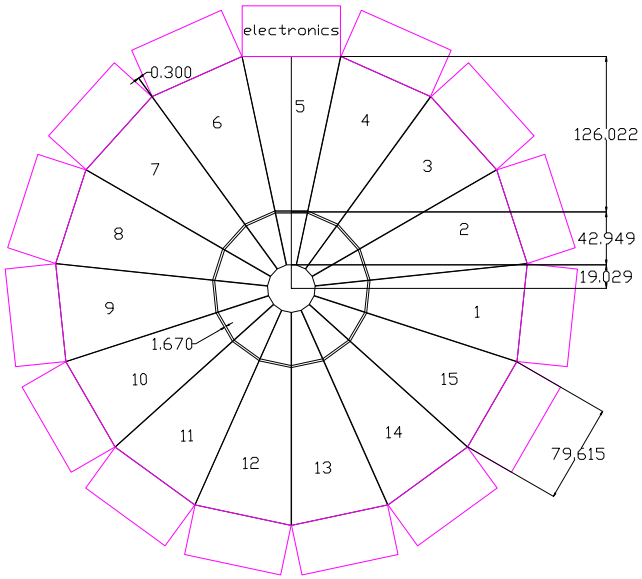

Figure 6: Front view of the first region of the FST showing the layout and positioning of the trapezoidal sensors.

In the critical region around the beam axis at r ~19 mm, because the sensors are trapezoidal, the V and the W layers of a region each have ~40 strips per sector, distributed over 2π, a total of ~600 strips per layer. The rate near the beam axis has to be handled by these 600 strips. Though 600 strips per layer around the beam axis appears to be a small number, the readout electronics associated with these strips will on average have a rate-load of ~10 KHz that can be handled by the readout electronics.

3.5 Barrel Silicon Tracker (BST)

The four BST regions have ~240 mm of radial space available for tracking. Having four regions instead of the minimum three needed for track reconstruction provides a redundant tracking region that mitigates the risk of tracking inefficiencies due to layer problems such as malfunctioning strips, electronics, or noise. Further, tracking simulations indicate that with four regions instead of three, the probability of reconstructing fake tracks for a given number of correlated background hits per region (that are randomly distributed over the four BST regions) is reduced by a factor of three. Our simulations indicate that four regions should be able to handle about forty background hits in the time window. The first BST region

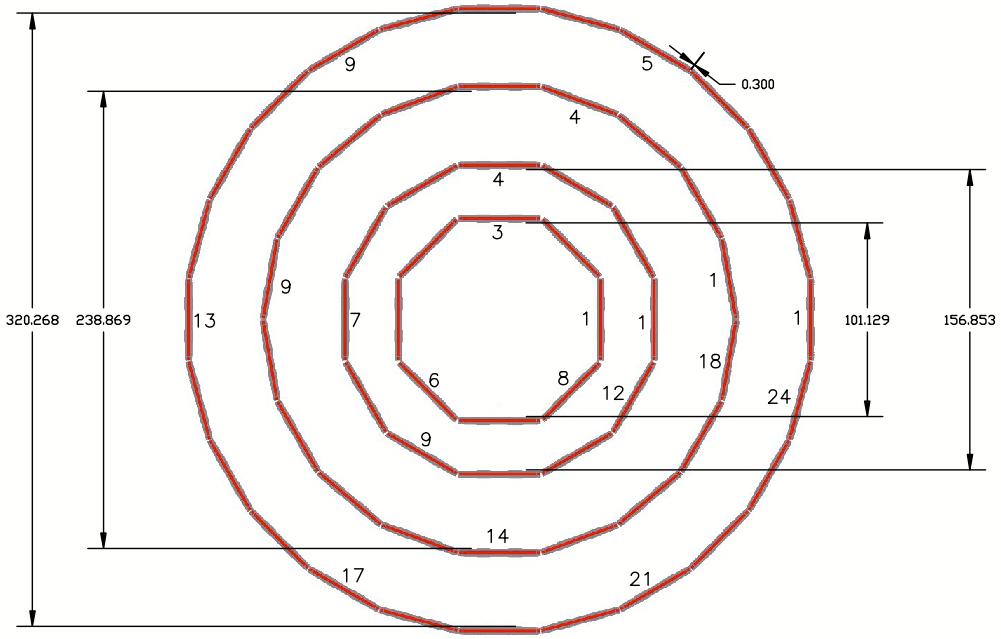

Figure 7: Rear view of the barrel section of the SVT showing the sensor partitioning in each region.

has a diameter of ∼101 mm. The second, third, and fourth BST regions have diameters of ∼157 mm, ∼239 mm, and ∼320 mm, respectively. The radial distance, Δr, between region four and region one of the BST has been chosen to maximize momentum resolution, which has an inverse square dependence on Δr. In ϕ, the BST regions, from the innermost to the outermost, are partitioned in 8, 12, 18, and 24 sectors, as shown in Fig. 7. Studies indicate that track loss due to the cracks between adjacent sectors in the BST is less than 5% for a half-field setting of the solenoid, as long as the cracks are no wider than 2 mm.

3.6 Dicing Layout

The dicing layout for a trapezoidal sensor from a 6-in diameter wafer is shown in Fig. 8. The dicing process demands a keep-out zone of 0.25 in around the edge of the wafer.

The BST dicing layout of a 6-in wafer, as shown in Fig. 9, is such that it provides the longest sensors possible. Such a layout reduces the number of sensors needed for the BST modules. Further, cost is reduced by maximizing the yield of sensors from a single wafer – minimizing the total number of wafers required for the BST. All BST regions use sensors with a cut size of 111.62 mm × 42.00 mm × 0.300 mm.

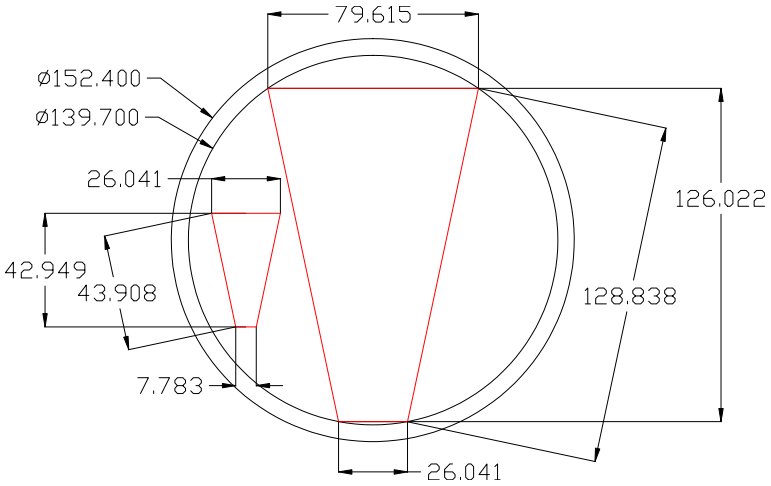

Figure 8: Trapezoidal sensor dicing from a standard 6-in wafer. All units in mm.

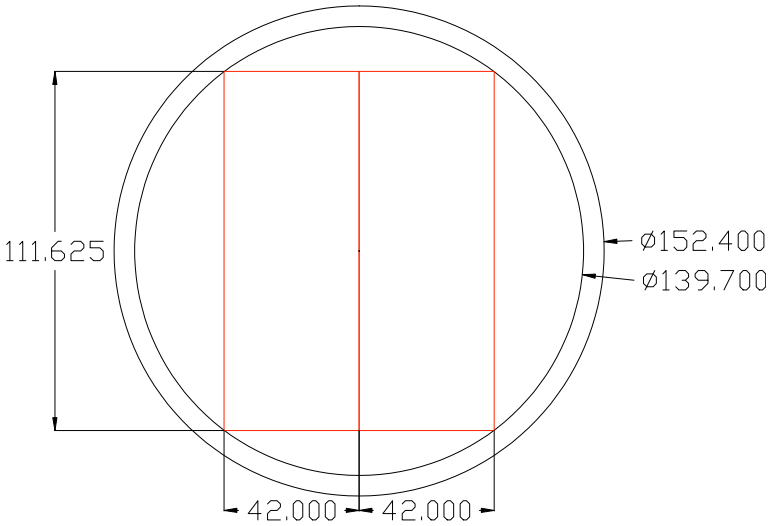

Figure 9: Barrel sensor dicing from a standard 6-in wafer. All units in mm.

3.7 Module and Strip Layout

Fig. 10 shows the cross sectional view of the sensor. The lengths of the readout strips of the SVT vary from 0.5 cm to 33 cm. The strip width is ∼8 μm and the implant depth ∼1.2 μm.

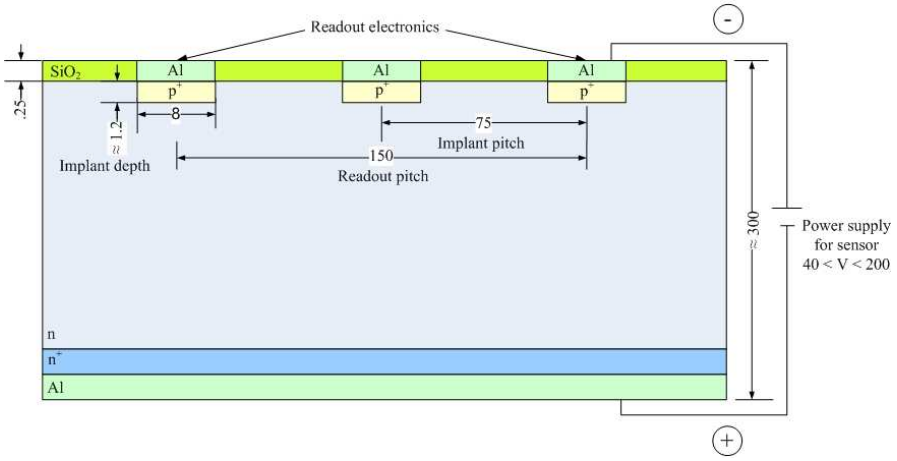

Figure 10: Cross sectional view of a sensor showing the different layers and the spacing of the strips (all units in μm).

A completed module in the BST has 256 readout channels per layer – 512 channels in all per module. The modules of the FST have 512 channels per layer – 1024 channels total per module. Each FST sector consists of a module – a single trapezoidal unit as shown in Fig. 8 that consists of a V and a W silicon layer that sandwich a 2-mm-thick Rohacell 71 carbon fiber composite.

To reduce costs, the V and W layers for the modules of the different BST regions are made of one or more fundamental rectangular sensors. If more than one sensor is needed for a module, the sensors are wire-bonded together. Modules of the BST Regions 1, 2, 3, and 4 have 1, 2, 3, and 3 sensors, respectively (see Fig. 4). Fig. 11 shows 3D renderings of how the complete SVT system is expected to look.

Table 2 gives the radiation length of the materials used for the sensor structure. Because of the large variety of commercial graphite fibers available for GFRP (glass fiber reinforced polymer) composites, they have an added bonus of being easily obtainable at an acceptable cost. The preferred structural materials are GFRP and Rohacell. The total anticipated radiation length for the BST is ∼3.5% and for the FST ∼2.7%.

The readout pitch for the strips, which is twice the implant pitch, is determined by the minimization, as far as affordable, of spatial resolution. Based on this criterion, the strips

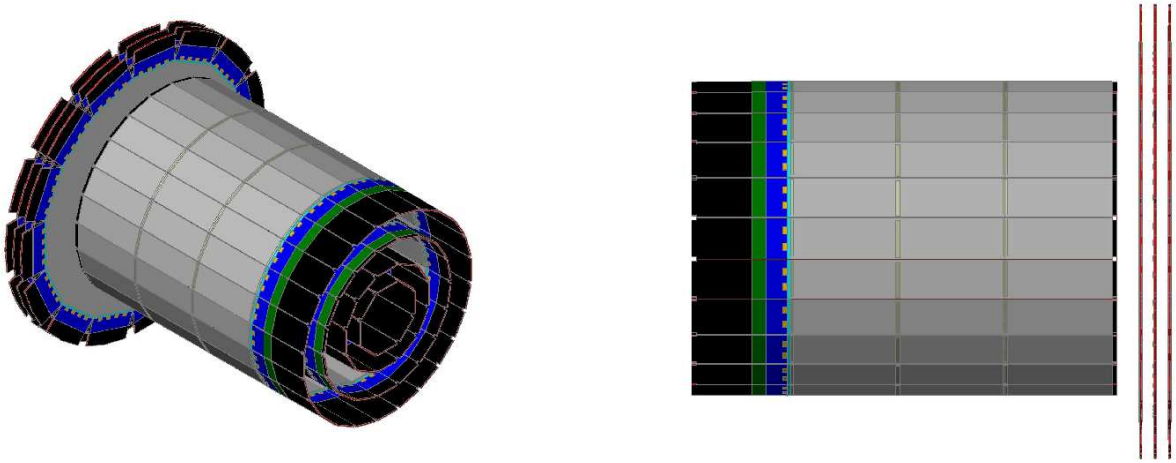

Figure 11: Overall conceptual renderings for the SVT showing a rear view (left) and a side view (right).

Material	Radiation Length (mm)	Thickness (mm)	Radiation Length [%X0]
Silicon	93.7	0.300	0.320
Epoxy	443.7	0.025	0.007
GFRP	250.0	0.250	0.100
Rohacell71	5450.0	2.000	0.040
GFRP	250.0	0.250	0.100
Epoxy	443.7	0.025	0.007
Silicon	93.7	0.300	0.320

Table 2: Material thickness with radiation lengths for the different layers that make up the sensors of the BST and FST.

are designed to have an implant pitch of 0.075 mm and a readout pitch of 0.150 mm. The expected spatial resolution for this pitch spacing is about 0.050 mm and the occupancy in a layer of an FST region, for half-field operation of the solenoid, is less than ∼1.5%. The V and W layer strips for the FST sensors run parallel to the edges of the trapezoid (see Fig. 12), with the strips intersecting at an angle of 12°.

For the BST, the 42-mm width of the sensor accommodates 256 input channels, at a readout strip pitch of 0.150 mm, to the two SVX4 ASICs, and the required keep-out zones around the sensor (see Fig. 13). The V and W strips are designed such that strip 1 is at an angle of 0° with respect to the length axis of the rectangular BST sensors and strip 256 is at an angle of 3°. This was done to minimize sensor dead area. Details are shown in Fig. 13.

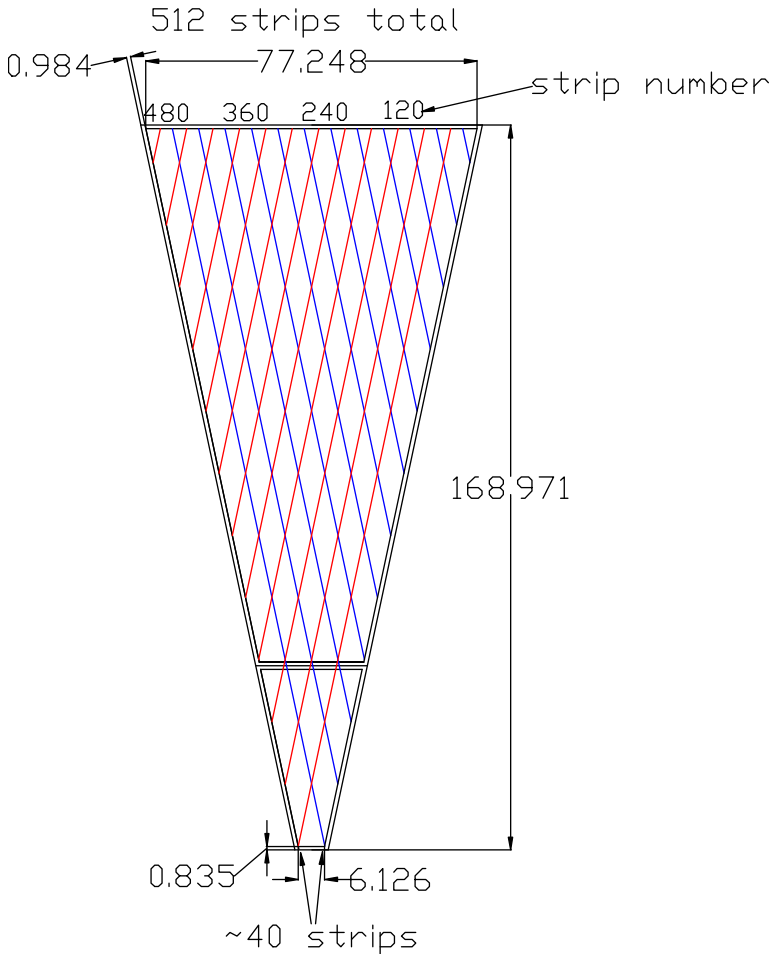

Figure 12: Strip layout for the trapezoidal sensors. All units in mm.

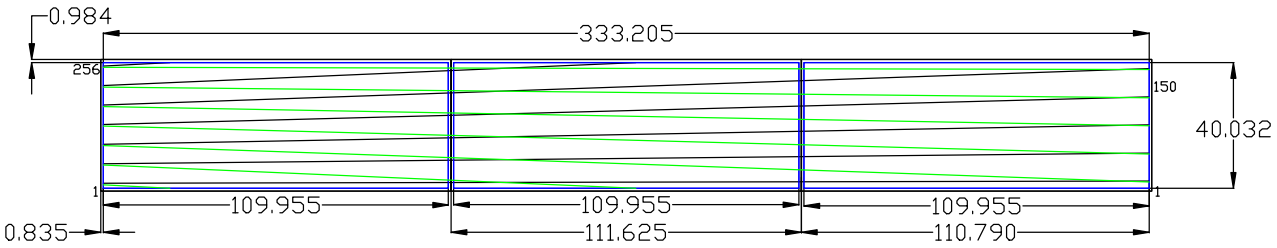

Figure 13: A standard BST module showing the V and W strips. All units in mm.

4 Mechanical

4.1 Support Structure

Fig. 14 shows a view of the complete SVT, including its support structure. A large stainless-steel tube is used to support the BST, and the FST is supported off of the BST. The size and stiffness of the support tube seems extreme, but it is a simple system that has been used to support other detectors in high magnetic fields in CLAS experiments, such as the light-weight BONUS detector. It is expected that the total weight of the SVT is less than 10 kg. The calculated deflection of the support pipe is 0.033 mm.

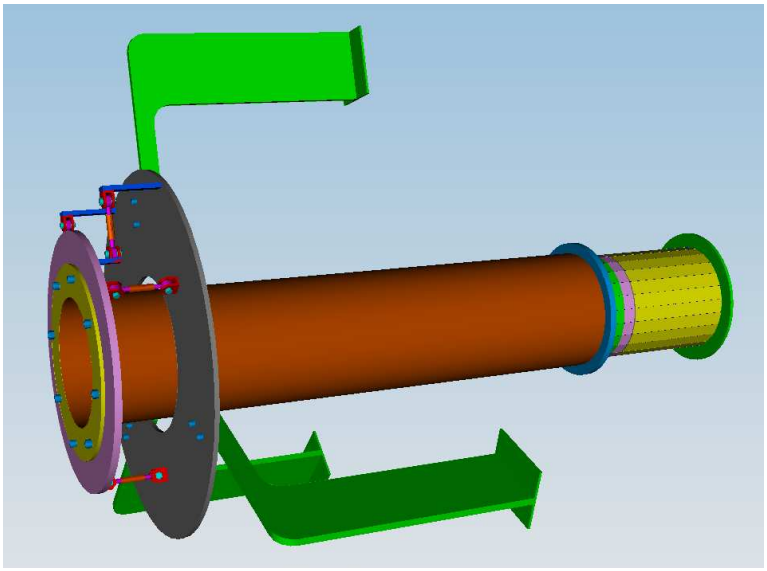

Figure 14: SVT on support arm with mounting/alignment hardware to CLAS12 solenoid.

The relative mass of the support structure is more than 5 times the mass of the detector, and it is mounted to the solenoid, which has a mass on the order of 20 metric tons, thus vibration will not be an issue.

4.2 Detector Element Deflection

Individual staves of the barrel section have been analyzed using ANSYS finite element modeling software. The worst case is Region 1, where its deflection is shown in Fig. 15. In this modeling, all elements of the stave were given both density and stiffness properties, as well as the dead weight of the electronics (10 g). Deflection of the wafer material can be seen to be less than 0.03 mm, which is much less than the required 0.1 mm that can cause self induced noise.

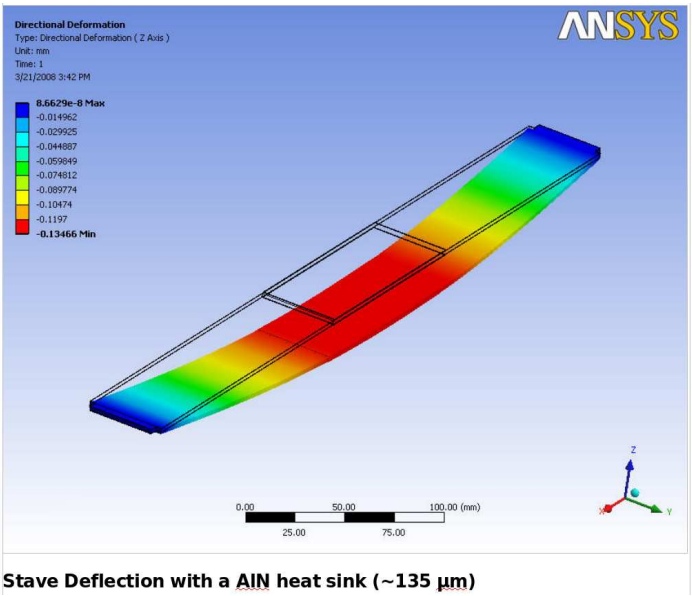

Figure 15: BST Region 1 stave deflection analysis results (units in mm).

4.3 Detector Element Heat Removal

Heat removal from the SVT is a significant design issue. The design heat load for the SVT is to remove all the on-board electronics heat using chilled-water cooling. The total power to be removed is shown in Table 3.

The primary mode of heat transfer will be conduction heat transfer to a water-cooled heat sink. We have chosen aluminum nitride because it is a non-magnetic and electrically non-conductive ceramic material with good thermal conductivity. Two millimeter thick aluminum nitride has been put into the core of the staves, replacing the Rohacell core material where its mass is not in the acceptance. Finite element analysis of a Region 4 module shows that

Heat Load for SVX4		
Item	Barrel	Disk
No. of modules	62	45
Chips/module	4	8
Total chips	248	360
Idle power (W)	47.6	69.1
Max power/ch (mW/ch)	3	3
Max power (W)	95.2	138.2
Transceiver power (W)	0.5	0.5
No. of transceivers/module	4	4
Total transceiver power (W)	124.0	90
Total idle power (W) (with transceiver)	171.6	159.1
Total max. power (W) (with transceiver)	219.2	228.2

Table 3: Heat load on the SVT,

most of the heat can be conducted away, keeping the electronics maximum temperature to approximately 40°C with the heat sink temperature at 15°C. A very small amount of heat (much less than 1 W) must be removed from the surface of the wafers to keep them from warming to the maximum temperature of the chips. This can easily be done by flushing the detector with a small purge of dry nitrogen. The temperature distribution of a stave in Region 4 is shown in Fig. 16.

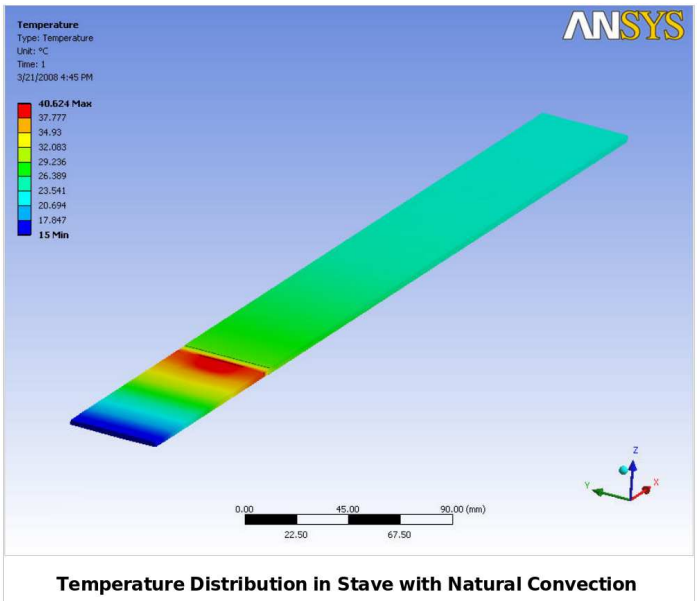

Figure 16: BST Region 4 stave heat transfer analysis results (units in °C).

Notice that the temperature along the wafer portion of the stave is around 23°C. This is because the dry nitrogen that will be purging the detector is assumed to be 22°C. Region 1 has a longer conduction length, and therefore, higher temperatures are expected. Two potential solutions are being considered. The first is to use a material with higher thermal conductivity (such as a high thermally conductive carbon composite). The second is to locate the electronics on Region 1 closer to the cooling plate.

5 Electronics

5.1 Readout

Both the BST and FST will be made of single-sided sensors, as single-sided sensors avoid manufacturing problems and the higher costs associated with double-sided sensors. Further, the

SVX4 ASIC, a candidate for the readout electronics, supports single-sided sensors only. The single-sided sensors to be used are n-type, AC-coupled, and poly-biased. After an evaluation of the readout ASICs that are available (see Table 4), the 128-channel SVX4 ASIC that is fabricated on standard 0.25-μm CMOS technology, is considered to be a potential candidate. SVX4 implements a complete readout system and is a low-power device (at 3 mW/channel). Further, the SVX4 ASIC has a good track record and is presently the readout system of choice for several single-sided micro-strip detectors.

Institution	Experiment	Chip	Manufacturer	Process
CERN	ALICE	HAL25	IBM	0.25
CERN	ATLAS	ABCD	Honeywell	0.8
CERN	CMS	APV25	IBM	0.25
CERN	LHCb	BEETLE	IBM	0.25
FNAL	CDF	SVX4	TSMC	0.25
FNAL	D0,CDF	SVX3D	Honeywell	0.8
KEK	Belle	VA1TA	IDEAS	0.35
SLAC	BaBar	AToM	Honeywell	0.8

Table 4: Available ASICs that were evaluated for use in `CLAS12`.

As an example of the on-board electronics, a photo-composite of a BST Region 2 module is shown in Fig. 17. This assembly is called a stave. Table 5 lists the significant components of the on-detector electronics. The operating bias voltage is expected to be $\sim$200 V. For low thermal noise and production uniformity, the poly-silicon bias resistor is required to be $\sim$2.5 MΩ. The inter-strip resistance is expected to be $\sim$1 GΩ. To minimize signal dispersion, a strip resistance of less than 30 Ω/cm is desirable.

The SVX4 design handles sensor capacitances from 10 pF to 35 pF. For the FST and the BST, the total inter-strip capacitance is expected to be $\leq$1.2 pF/cm and the coupling capacitance is expected to be $\geq$10 pF/cm for AC-coupled strips. The equivalent noise charge (ENC) in a channel is given by ENC = $400e^- + 42e^-/$ pF. For a capacitance of 30 pF, the typical capacitance of a long strip, plus some additional stray capacitance due to the wire-bonds connecting the sensor and the chip, ENC is estimated to be $1800e^-$. This noise level is about a tenth of the signal level generated by a minimum ionizing particle.

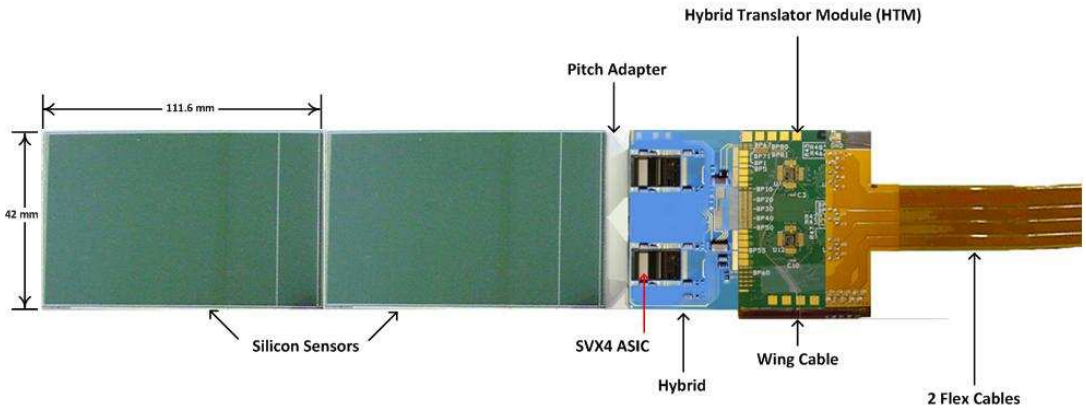

Figure 17: Photo-composite of a Region 2 barrel module stave assembly.

Component	Basic Specifications	Function
Silicon sensors	Single sided, 300-μm thick, 42 mm×111.62 mm (cut), 75 μm implant pitch, 150 μm readout pitch, V/W layers $\pm 1.5°$, n-type, 2 sensors from a 6-in wafer	Charge collection
Pitch adapters	Adapts SVX4 48-μm pitch to sensor 150-μm readout pitch	Hybrid to sensor Connection
Hybrids	BeO substrate, ~38 mm×20 mm, bonding pads for 2 SVX4 ASICs	SVX4 ASIC mounting
Hybrid Translator Module (HTM)	LVDS signal transceivers, ~40 mm×40 mm (smaller if possible)	Translates and repeats module control and data signals
Wing cable	Flex cable extension of HTM circuit board, wire-bond pads for bottom hybrid	Connects signals from top to bottom HTM

Table 5: Significant components of the on-board electronics.

Fig. 18 shows a block diagram of a single SVX4 channel. The detector signals are integrated, correlated double samples, the difference of which is stored in the analog pipeline. Up to 42 measurements can be stored in the pipeline. Digitization is by means of a Wilkinson-type ADC and an 8-bit counter. Timing control signals govern, among other functions, the operation of each channel's preamp reset, the double-correlated sampling, and the ADC. These timing control signals must be generated by a trigger generated by other detectors in `CLAS12`. Once a pipeline cell is marked by the level 1 accept (L1A) trigger, the counter value is stored in a FIFO buffer. An 8-bit output bus transmits the data in a sequence of bytes identifying the chip, pipeline cell, the channel number, and the content.

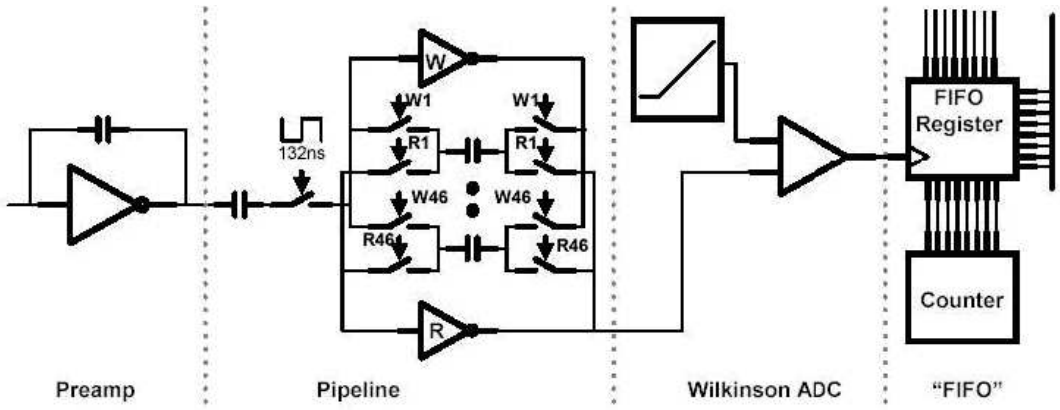

Figure 18: Schematic of an SVX4 chip showing the layout for the preamp, through the pipeline and ADC to the FIFO buffer.

Fig. 19 shows the floor plan of the SVX4 ASIC. The thickness of the chip is 0.25 mm. The diced area of the chip is 6.40 mm $\times$ 9.11 mm. The channel input pads are 0.096 mm apart, center-to-center, and the pad widths are 0.048 mm. There are two rows of input pads to which the outputs of the silicon sensors have to be wire-bonded. Pitch adapters connect the sensor and the hybrid. Wire-bond pads are located on both ends of the pitch adapter for connections to the SVX4 ASICs and to the sensor. The wire-bonding pads will be compatible with the aluminum-wire ultrasonic wedge-bonding method. A separate ceramic pitch adapter will be glued onto the module support assembly. Fig. 20 shows the pitch adapter connections to the sensor and SVX4 ASICs. Fiducial marks will be made on the pitch adapter for assembly and alignment. In addition to routing the sensor signals and the guard ground, the high voltage will be routed across the pitch adapter from the hybrid to the sensor bias ring. Adequate spacing between the pitch adapter, high voltage trace, sensor guard, and ground will be provided.

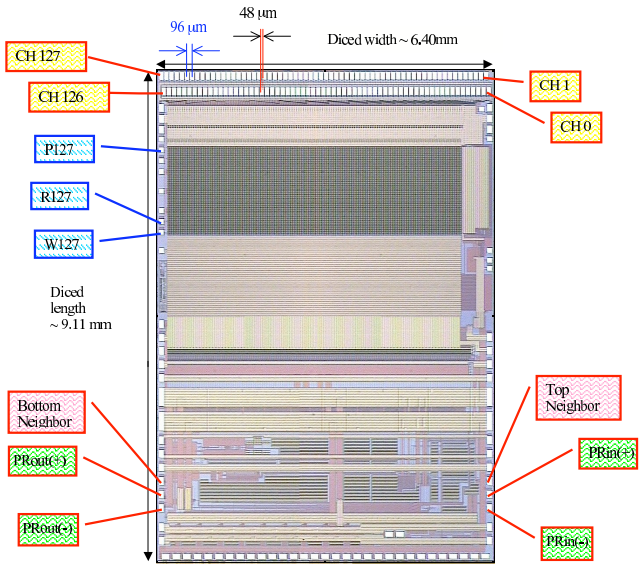

Figure 19: SVX4 ASIC floor plan.

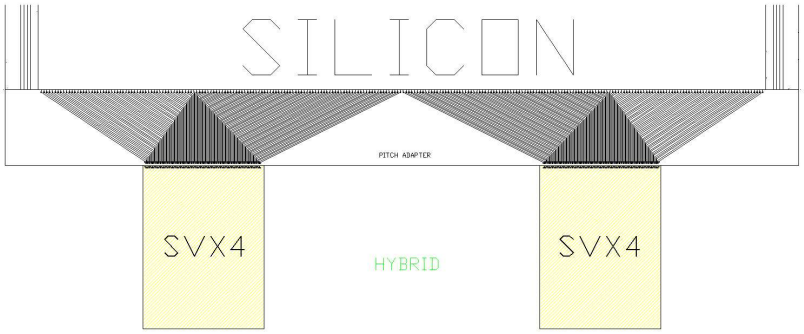

Figure 20: Pitch adapter connections to the sensor.

Fig. 21 shows a photo-composite of the proposed hybrid for mounting the SVX4 chips. The hybrid will be outside of the active area, not on the sensor, and glued directly onto the support structure. The proposed hybrid with approximate dimensions of 38 mm × 20 mm will be used to mount the two SVX4 readout ASICs. The hybrid substrate uses beryllium oxide, which is a good heat conductor and has a long radiation length. The gold bond pads of the hybrid will be aluminum-wedge bondable to be compatible with the other components. The high voltage for the sensors will be routed across the hybrid with an adequate wire-bonding surface for connections to the pitch adapter and the hybrid translator module (HTM). An RTD (resistance temperature detector) will be mounted on the hybrid for temperature measurements.

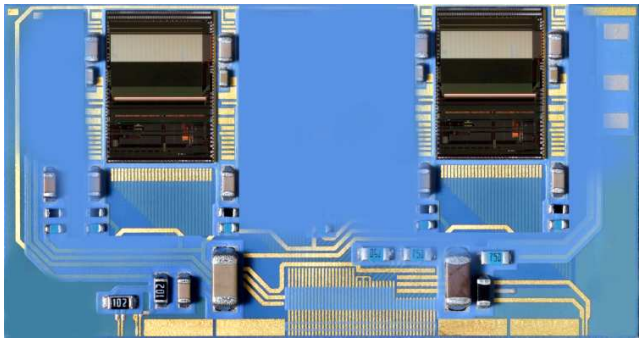

Figure 21: Photo-composite of the hybrid board for mounting of the SVX4 chips.

Separate power supplies and grounds for the analog and digital sections will be used. The dielectric strength of the circuit board will be ≥650 V/mil. SVX4 diagnostic signals have external pull-up resistors and will be routed to the hybrid test points. Fig. 22 shows a conceptual schematic of the hybrid based on the FNAL CDF design.

The connections for the priority in - priority out SVX4 readout chain allow for reading the top side and then the bottom side of the module. The input and output for the readout chain are then routed to HTM transceivers and then to the external connectors. The HTM translates and repeats control and data signals from the two hybrids on a module to the DAQ. The HTM also routes the low voltage and high voltage supply lines from the flex cables to the hybrid. Fig. 23 shows a conceptual block diagram of the SVX4 readout chain. Fig. 24 (top) shows a FNAL HTM that has the dimensions of 39 mm × 50 mm; at JLab a smaller module (∼40 mm × 30 mm or less) is being developed for `CLAS12`. Fig. 24 (bottom) shows a block diagram of the HTM board. The FNAL 10-bit low voltage differential signal ASIC

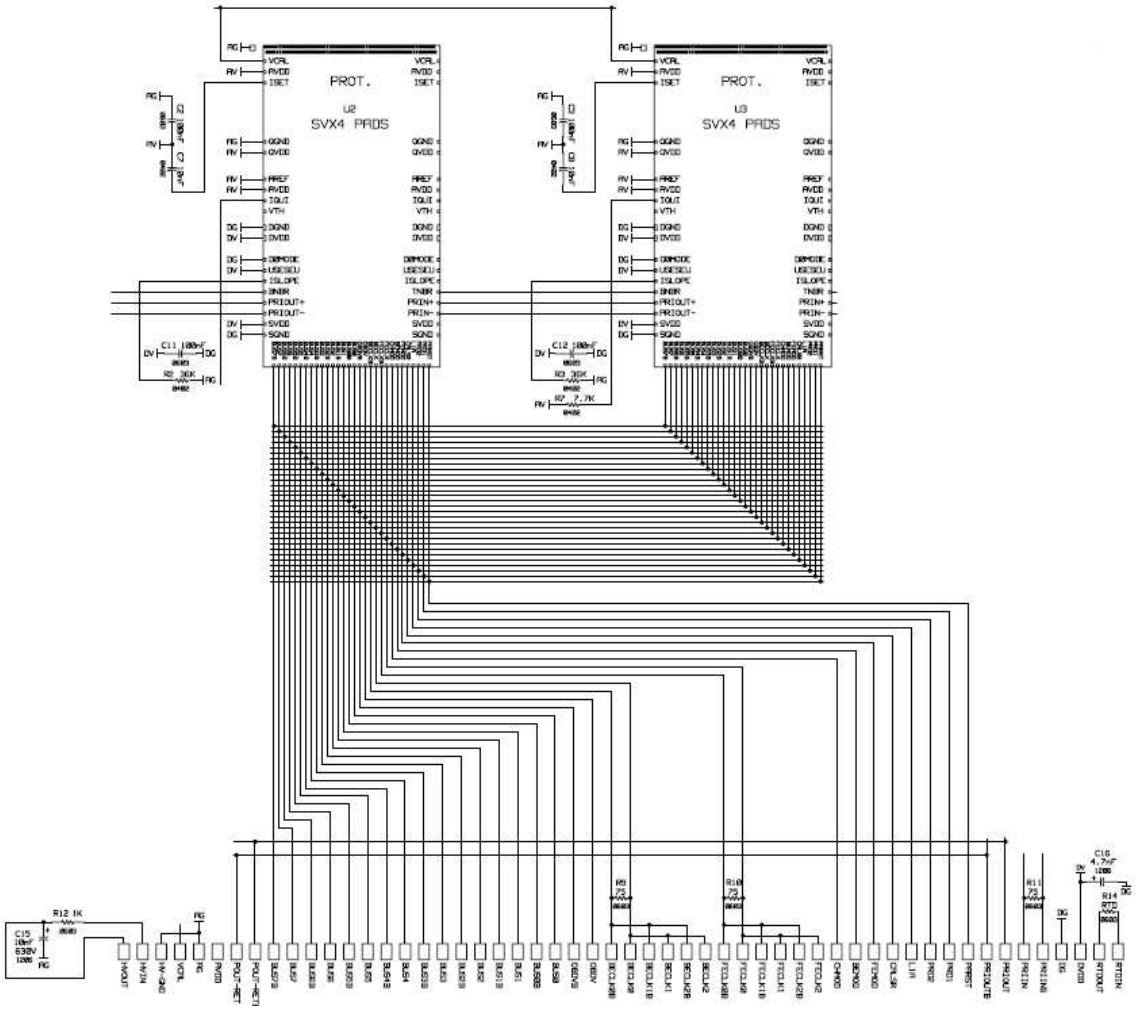

Figure 22: Conceptual schematic of the hybrid board layout of the SVT.

transceiver will be used because of its high density and its good track record with silicon-strip detectors. The transceiver comes in die form and is wire-bonded to the HTM board.

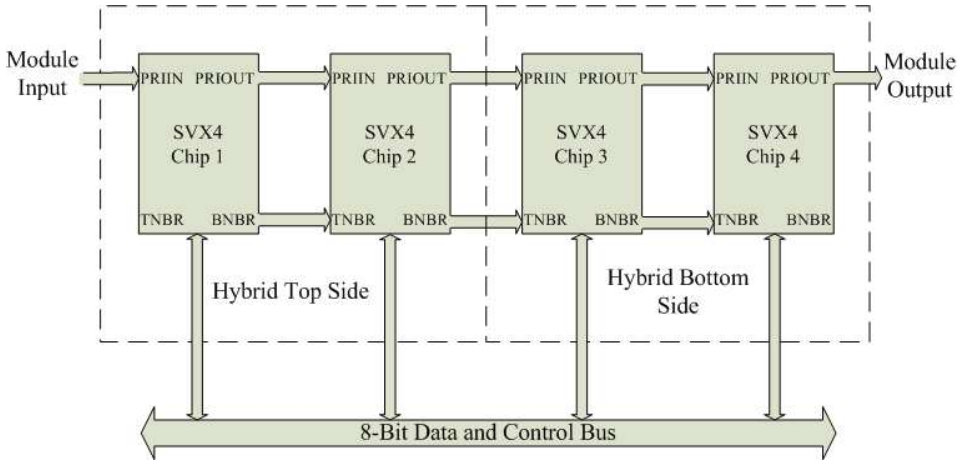

Figure 23: SVX4 readout chain configuration.

The "wing" cable connects the bottom-side hybrid to the transceiver on the HTM board. The wing cable and the HTM will be combined together into a single polyimide rigid (HTM) and flex (wing cable) assembly. In addition to the wing cable, the two flex cables with the data, low voltage, and high voltage connectors will be attached to the HTM board. Fig. 25 shows the wing cable on bottom side of the module. Fig. 26 shows the HTM board and wing cable before folding. Fig. 27 shows the flex cable assembly. The length of the cable is limited to ~30 cm. Fig. 28 shows the flow of the cables. All cables will be routed to the electronic racks located at the rear of the detector.

5.2 High and Low Voltage

The system is designed with the highest low voltage and high voltage segmentation affordable, without compromising performance and operability. Each side of the module has its own high voltage channel, two high voltage channels per module. The five channels of low voltage for the module consist of a hybrid analog and a hybrid digital channel for the top and for the bottom sides of the sensor module and a digital channel for the HTM. All of these channels operate at 2.5 V. In addition to the low voltage and high voltage, a calibration voltage for each of the two hybrids connects to the flex cable low voltage connector.

The low voltage system consists of ~625 channels in four groups. The high voltage system has ~240 channels. Fig. 29 shows the distribution of voltage and monitoring channels for the

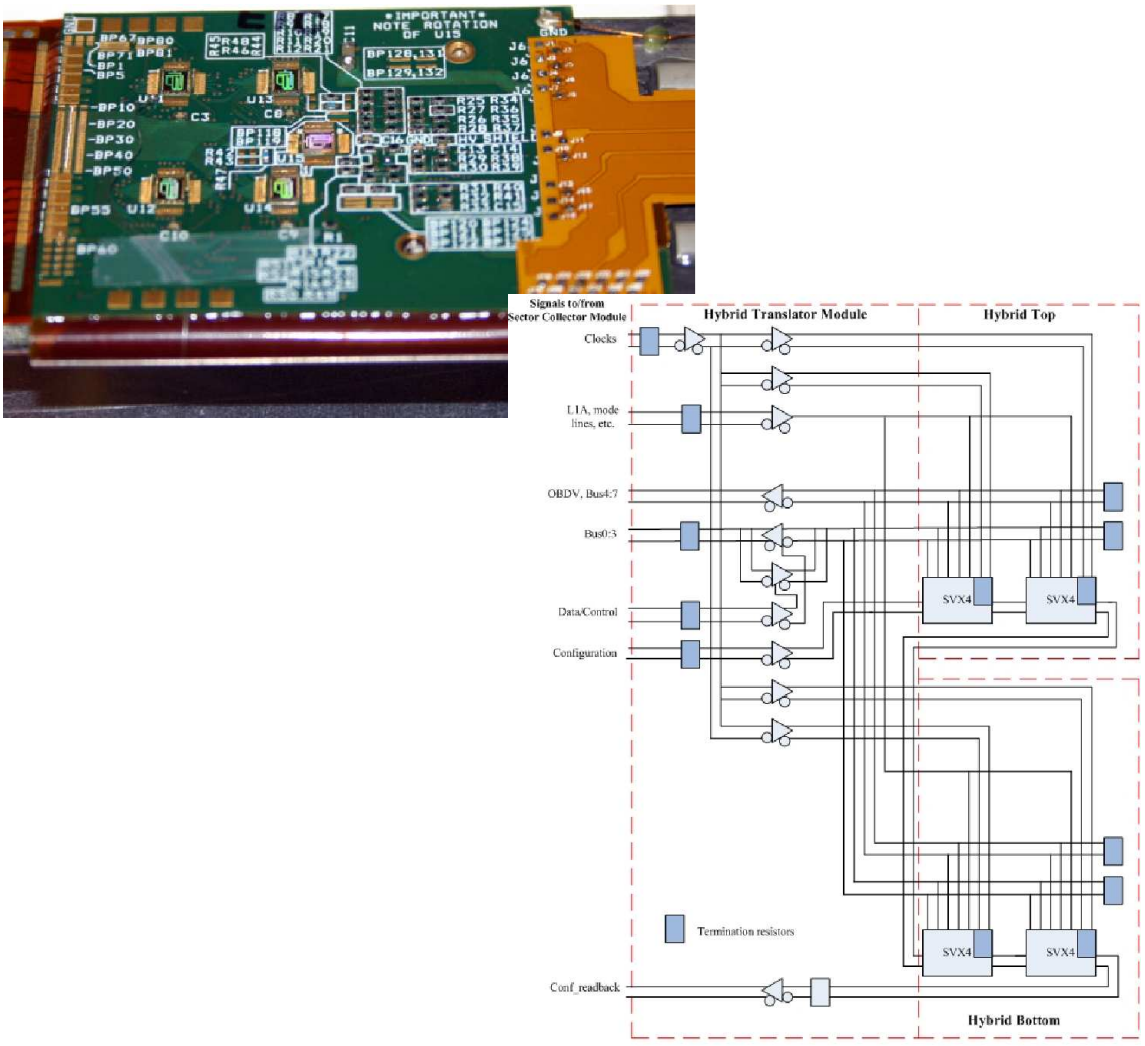

Figure 24: (Top) Top side view of the hybrid translator module (HTM). (Bottom) Corresponding block diagram for the HTM board.

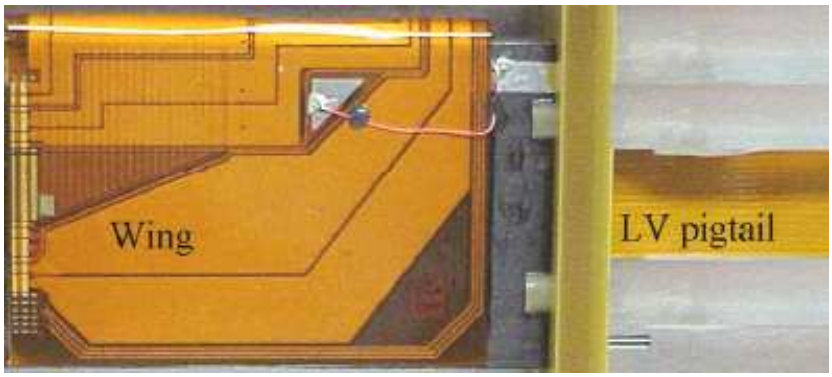

Figure 25: Wing cable on the bottom of the HTM board.

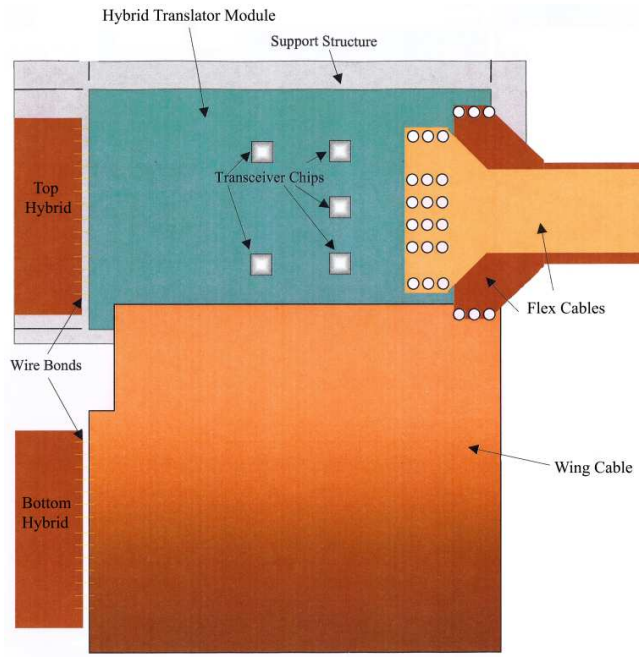

Figure 26: HTM assembly showing the wing cable to connect the top and bottom side boards and the readout flex cable.

Figure 27: Photograph of the flex cable assembly.

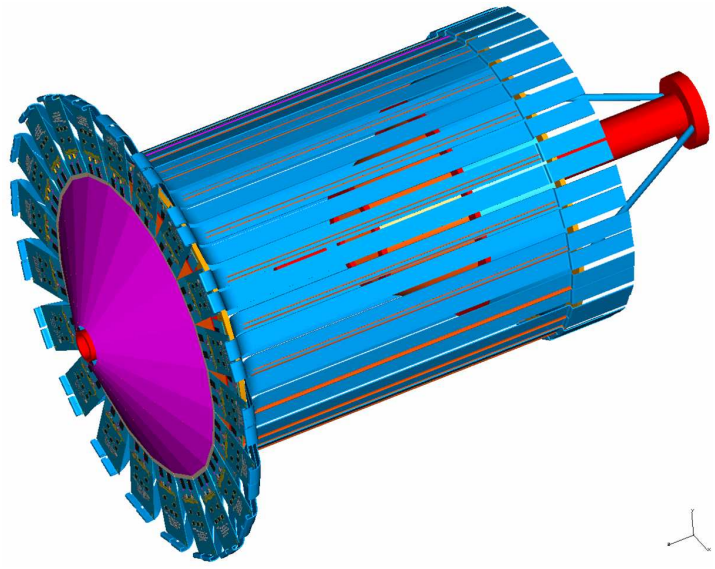

Figure 28: Cable routing diagram for the SVT detector.

SVT. The low voltage and high voltage supplies for the SVT will be modular with individual channels provided by a module within a main supply crate. Sensors will have a controllable and monitorable high voltage channel with over-current and over-voltage trip protection. A calibration signal and a temperature sensor on each hybrid will be instrumented on the detector modules. Table 6 shows the distribution of low and high voltage channels needed for the sensors, the HTMs, and the sector collector modules (SCM).

The CAEN crate-based high voltage systems, including the 1527 and 1527LC, and the WIENER universal multi-channel modular system for both low voltage and high voltage supply are being considered. The WIENER modular system has the advantage of a common crate that will support both high voltage and low voltage modules. Fig. 29 shows an overview of the connections of the system.

5.3 Slow Controls

Calibration and testing of the detector modules and readout chain is accomplished by a calibration input signal (VCAL). This external input on each SVX4 ASIC has the capability of injecting a small charge via a charge injection capacitor (25 fF). This capacitor can be switched in from each preamp input to a common bus line. A 128-bit programmable channel register, downloaded in the initialize mode, can function as a mask register and determine

Specification	Region 1	Region 2	Region 3	Region 4	Total
Hybrid 2.5 V digital channels (barrel)	14	24	34	44	116
Hybrid 2.5 V digital channels (nose cone)	40	42	42	0	124
Hybrid 2.5 V analog channels (barrel)	14	24	34	44	116
Hybrid 2.5 V analog channels (nose cone)	40	42	42	0	124
HTM LV channels (barrel)	7	12	17	22	58
HTM LV channels (nose cone)	20	21	21	0	62
SCM LV channels (barrel)	2	3	4	4	13
SCM LV channels (nose cone)	4	5	5	0	14
HV channels (barrel)	14	24	34	44	116
HV channels (nose cone)	40	42	42	0	124

Table 6: High and low voltage channel distribution for the SVT.

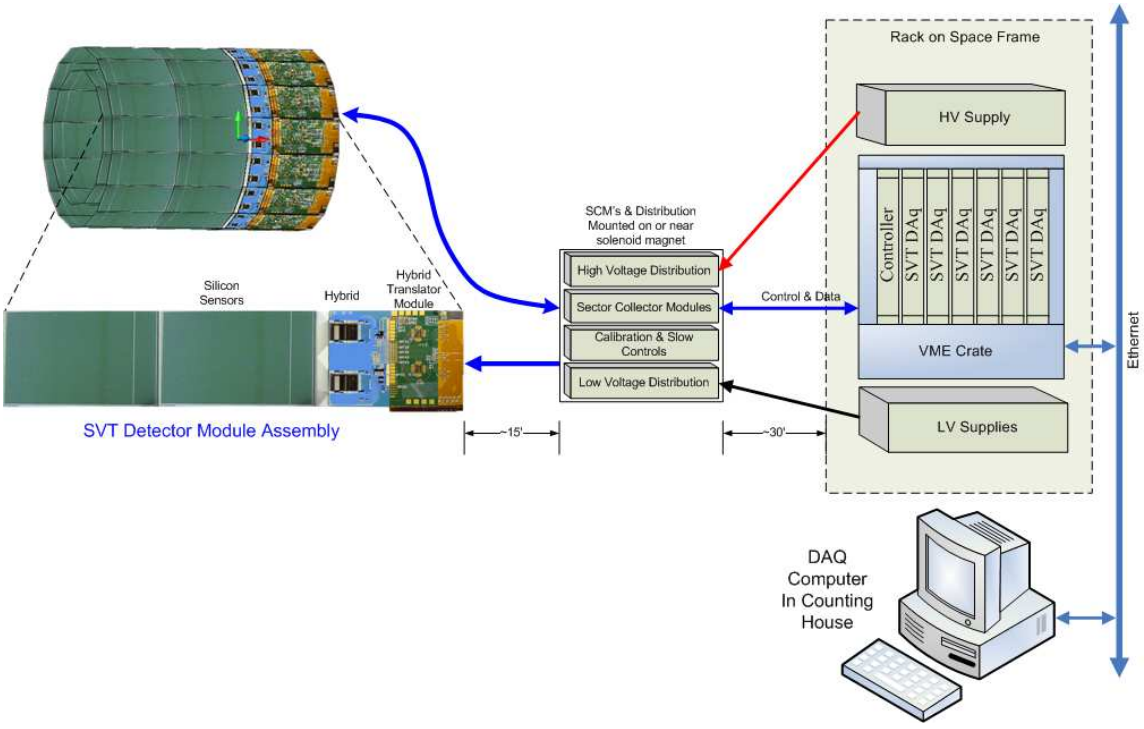

Figure 29: System connections overview for the SVT.

whether or not the injection capacitor is switched on for each channel. Fig. 30 (left) shows the preamp stage of the SVX4 ASIC and the VCAL calibration input.

The slow controls system (SCS) will be responsible for controlling all essential run-time parameters of the experiment and for monitoring the status of various hardware components. The primary goals are to enhance safety by providing early warnings about malfunctioning equipment and check the health of the experiment and the integrity of data. The system will also transmit important parameters to the DAQ for insertion in the `CLAS12` data stream. The SCS will have the ability to trigger alarms to notify personnel when parameters are detected to be outside pre-defined limits and will have the option of automatically disabling DAQ in case of a severe malfunction of the equipment. The implementation of the SCS will need a VME crate with an IOC and input/output boards. Some of the hardware will be connected directly to the Ethernet network. The settings of all critical operating parameters will be protected against computer failure. The failure of the computer in the system will only result in the loss of monitoring. When a computer reboots, parameters will not reset to previous or default values but remain at currently set values.

The SVT computers and vital support hardware will be protected by Uninterruptible Power Supplies (UPS) with battery backup and software to signal an alarm and notify the operators when external power is lost. The UPS will have surge protection and line filtering. Monitoring and control of the system will be implemented through the use of a Motorola single board computer embedded in a VME crate running VXworks real-time operating system. Sun or Hewlett-Packard workstations will support the user interfaces and controls. The control software will be built using the toolkit provided by the Experimental Physics and Industrial Control System (EPICS), which is based on the client-server model.

5.4 Data Acquisition

Each channel of the SVX4 ASIC has a 42-cell deep analog pipeline. Fig. 30 shows the block diagram of the ASIC. The front-end of the ASIC contains the integrator and storage pipeline, which at a front end clock rate (FEClk) of 132 ns, allows a trigger latency of $\sim$4 μs. The back-end of the ASIC has an ADC for digitization and the readout and driver logic.

The level 1 accept (L1A) signal to the ASIC is used to remove a "hit" cell from the pipeline. The hit is temporarily stored in a FIFO buffer that can store up to four cells, corresponding to four L1As. These hits are queued for readout to the back-end. Once four cells are stored

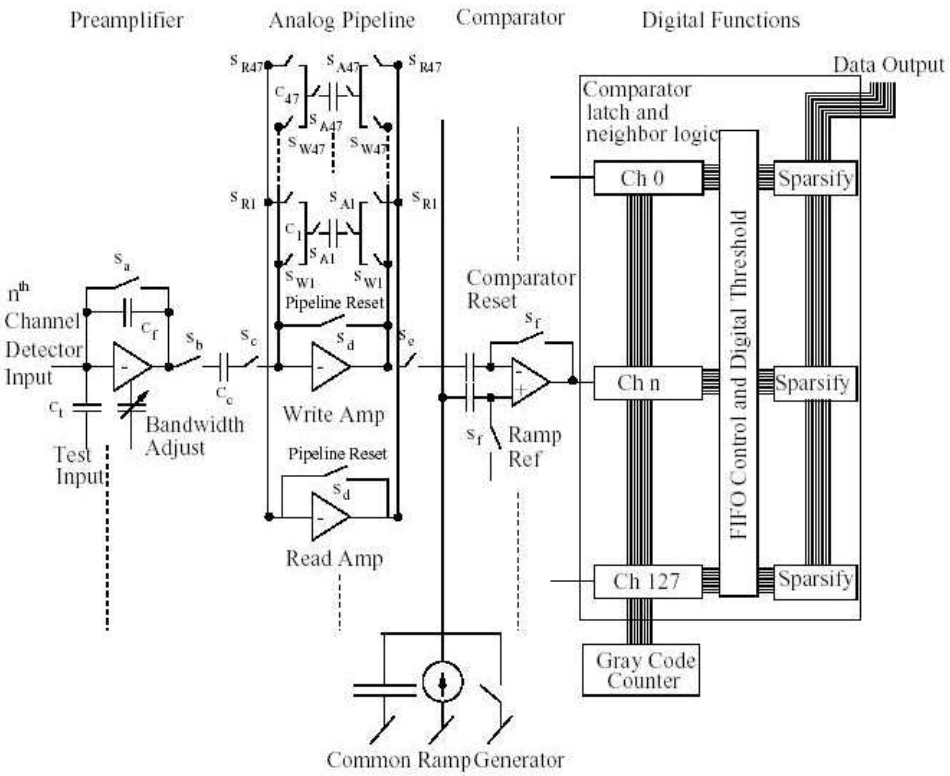

Figure 30: Block diagram of the SVX4.

in the FIFO, additional L1As are ignored. The trigger latency is programmed in the shift register during the initialize mode so that the right pipeline cell is read out. L1A is normally high during acquisition and pulsed low to store a cell. L1A must go low and return high between front-end clocks.

The pedestal pipeline cell is reserved for acquiring only pedestal data. This cell is used during readout along with a stored cell. The back-end digitizes the difference between the hit cell and the pedestal cell. The pedestal cell is not part of the round robin ensemble of acquisition cells, hence the pedestal cell must be refreshed periodically. Because of the continuous electron beam, L1A arrivals are not synchronized to the front-end clock, which implies that the associated detector signals are Poisson-distributed with respect to this clock.

SVX4 data acquisition rates at a luminosity of 1×10^{35} $cm^{-2}s^{-1}$ were simulated to check their performance in a continuous electron beam environment. The first aspect of the SVX4 that was simulated was the L1A acceptance rate [9]. The triggers generated were Poisson-distributed with respect to the SVX4s FEClk. The simulation estimated the number of triggers that had an early arrival time and also estimated the number of triggers that were missed. The results of the simulation showed that for half-field operation of the solenoid, 2.5 T, with an L1A rate of 10 kHz, $\sim$0.1% of the triggers arrived early. No triggers were missed. The simulation was run for an L1A rate of 100 kHz as well, over ten times the expected trigger rate. For these conditions only $\sim$1.3% of the triggers arrived early and $\sim$0.3% triggers were missed.

Another simulation checked the effect of issuing a reset and the associated restore operation when the pre-amplifiers on the chip saturate [10]. In operating the SVX4, charge is accumulated on the pre-amplifier and this charge needs to be periodically reset when it reaches $\sim$200 fC. The results of these simulations show that at half-field of the solenoid, a $\sim$1% deadtime can be expected; at full-field operation the deadtime is $\sim$0.4%.

SVX4 is designed for daisy-chained operation. Daisy-chaining minimizes the number of bus and control lines required to operate the device. Fewer control lines means less space on the high density interconnect and less mass in the system. All the chips share a common communication bus and a common differential and back-end clock. Each chip has two pads that are used for communication between adjoining chips. After powering up the SVX4, the chip parameters must be downloaded before operation of the readout chips can begin. For each SVX4 chip, 198 bits must be downloaded into the internal registers.

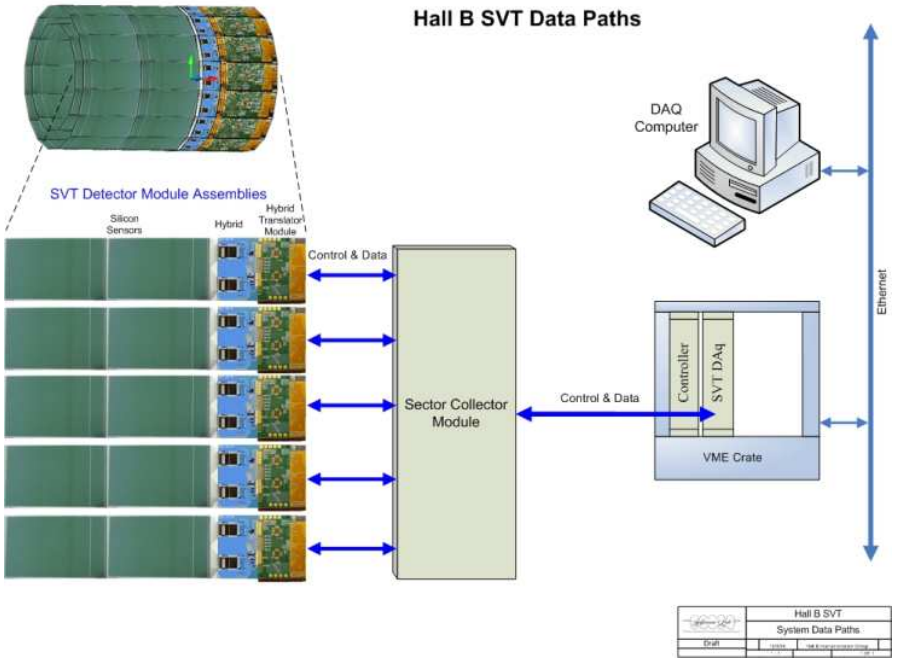

Figure 31: SVT system data paths.

Fig. 31 shows the data path for the Hall B SVT system. Signals are digitized in the SVX4 ASICs on the hybrids. The control signals and data bus for a module are connected to a sector collector module (SCM). Up to five modules are connected to an SCM that buffers and passes the data and control signals to the DAQ system. SCMs may also be daisy-chained together to form a longer readout chain. The readout chain requires only one detector module buffered by a single SCM to form a valid control and data path. Unused SCM inputs are bypassed. Increasing the number of SCMs connected together increases the daisy-chain length and the DAQ readout time. The fastest readout is accomplished by a single silicon detector module, SCM, and SVT DAQ module chain. Fig. 32 shows the daisy chain connections through an SCM.

For the `CLAS` upgrade, VME systems will be used for both DAQ and slow controls. Currently, `CLAS` uses about 30 VME crates and several types of modules. As a standard DAQ framework at JLab, 6U VME single board computers (SBCs) running VxWorks RTOS are used. The Harvard-designed Silicon Readout Controller (SRC) used in FNAL-CDF was studied for possible implementation in our system. This controller was originally designed for SVX3 readout. The CDF-SRC printed circuit board is in 9U VME format. This format is incompatible with our 6U-sized systems. The board has nine FPGAs and only controls the

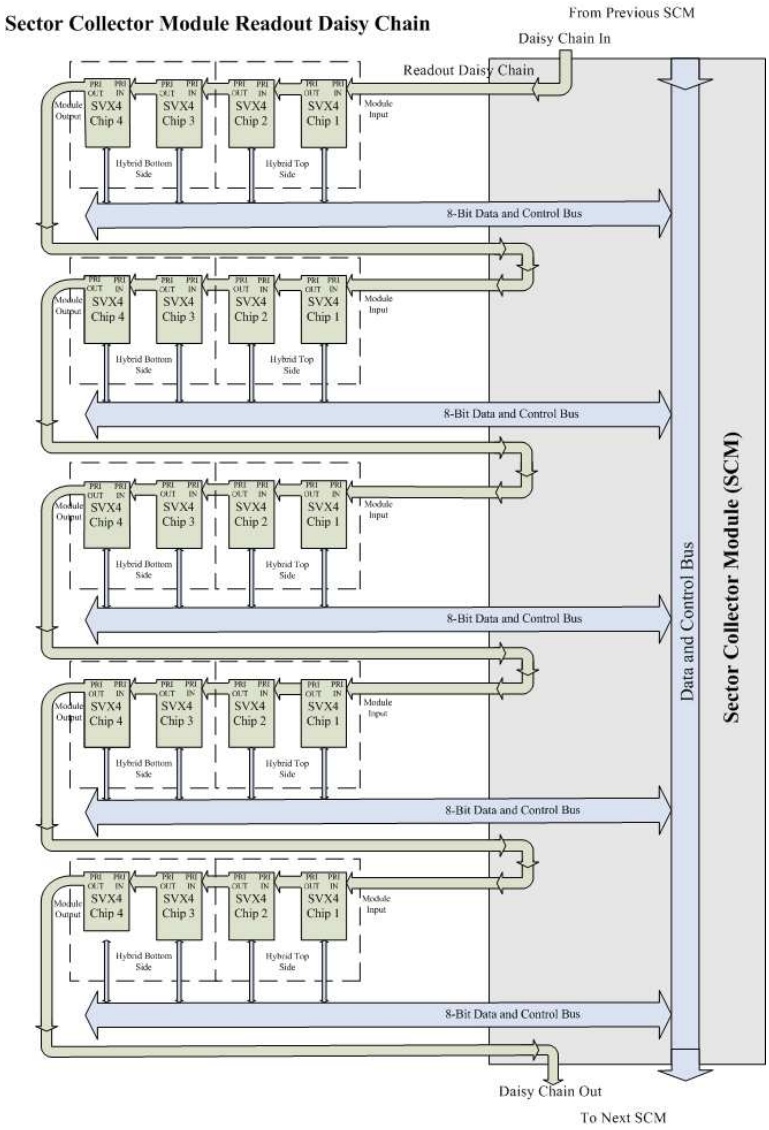

Figure 32: Sector collector module daisy-chain readout.

SVX3 ASIC. Separate VME hardware is needed to handle and store the data received from the silicon sensors. In addition, this SRC is application specific for the pulsed accelerator at FNAL and designed around the triggering system used at CDF.

For control and data acquisition for the SVT, a 6U VME board compatible with the `CLAS` data stream format is being developed [11]. This modular SRC will control and integrate the data received from the SVT readout chain into the DAQ system. Fig. 33 shows the block diagram of the prototype SRC. The heart of the SRC design is Field-Programmable Gate Arrays (FPGAs). The advantage of FPGA technology is that it combines the ease of software with the speed of hardware with permanent upgrade capabilities via downloaded updates. FPGAs have already provided the lab with versatile VME bus data acquisition and control interfaces. Current JLab FPGA designs provide control and monitoring for numerous systems by interfacing sensors and instrumentation with ADCs and TDCs. As shown in Fig. 33, data and control signals from the readout chain connect to the SVX4 controller FPGA logic for processing. Interface I/O signals are provided by the FPGA for external triggering, clock, and phase lock interfaces among others. The FPGA has a memory management unit and PCI interface that connects to the VME interface. On-board memory stores the events to be read out. The VME slave interface completes the data and control path to the VME backplane through bus transceivers.

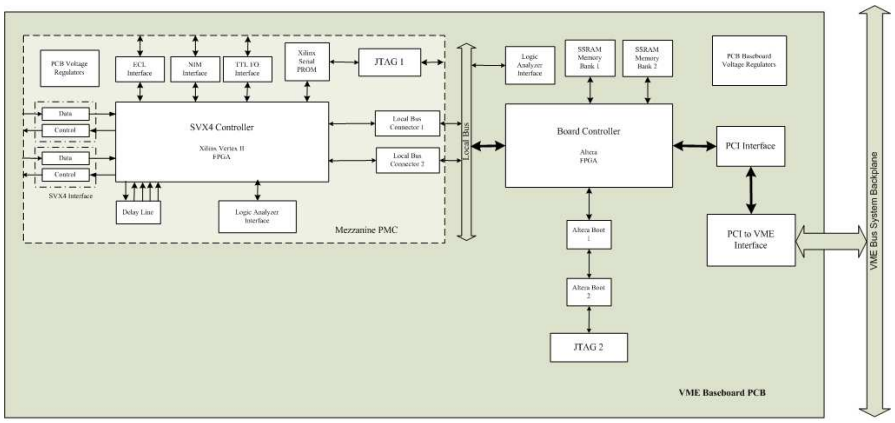

Figure 33: SRC prototype block diagram.

The SRC generates initialize, acquisition, digitization, and readout timing sequences for the SVX4 ASIC. The initialization cycle is typically performed once, followed by repetitive data acquisition, digitization, and readout sequences. Since we will be operating the SVX4 ASIC in continuous data format mode, the acquisition cycle occurs simultaneously with the

digitize and readout sequences. After the hit cell has been digitized in the SVX4, the SRC starts a readout cycle and the event data is stored locally. The event data will be continuously stored until the SRC is instructed to read out the data by the VME system controller or until the local memory is full. The VME slave interface on the SRC accepts instructions from the VME SBC. These instructions control the SVX4 sequences and read out the stored events. The SRC status register reports on the operating condition of the board including memory overflow.

The SRC design includes a Joint Test Action Group (JTAG) interface that provides In System Programming (ISP) capability. The ability to reprogram the on-board components provides a permanent upgrade path via software updates. It also provides a way to implement new features (even remotely) into an existing system after fabrication and installation. In addition, JTAG technology can be used for board level interconnection and functionality testing.

Based on the GEANT3 simulation, approximately 16 particles will be generated per trigger in the cone part of the SVT when the solenoid is operating at half-field. The forward cone is split into four groups, three of which have six modules and the last group has four modules. The four group partition results in four tracks per group per trigger. Six modules have 24 ASICs in all. For each chip, the pipeline cell and ID has to be read; this contributes 96 bytes, whether or not there is data. Four tracks in a group give rise to 6 hits, each of which requires a byte for cell ID and a byte for content, contributing 12 bytes per track. Therefore there are 48 bytes per track from hits alone. Therefore, there are 144 bytes per trigger. Since the groups are independently read out, this data rate translates to 1.44 MB/s for a trigger rate of 10 kHz, well below the 56 MB/s readout rate capable by the ASIC. Our expectations for the time taken for digitization and readout as a function of the number of hits in a sector of the FST have been computed and are shown in Fig. 34. Each sector can handle up to 2500 hits in 105 ns (25 MHz). A higher rate implies that before the digitization process can be completed a new L1A arrives, eventually filling up the FIFO and leading to a loss of triggers.

6 Research & Development

R&D for the SVT system started in FY2004 [12]. The R&D goals are to evaluate silicon strip detector systems, assess compatibility of SVX4 performance with `CLAS12` requirements, study

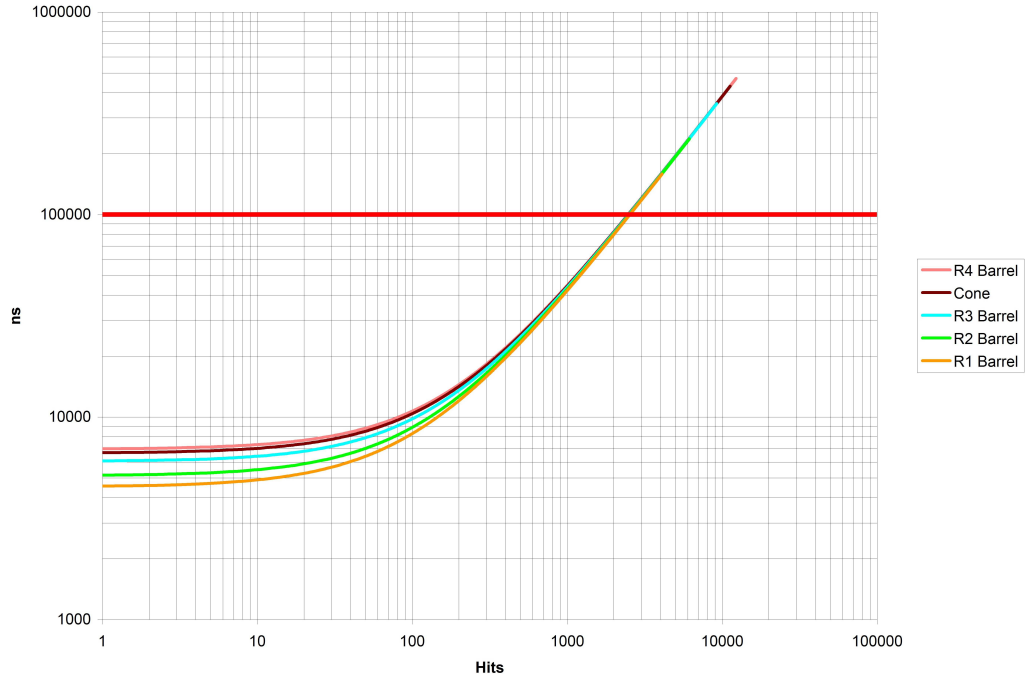

Figure 34: Readout time as a function of the number of hits in a given layer or portion of the SVT.

the features of the FNAL stave design that could be useful for CLAS12, and gain experience and know-how about developing support fixtures, installation, and DAQ by conducting lab tests and installing a test stave in Hall B for in-beam tests [5].

The initial R&D effort [13, 14] focused on the DAQ system of the stave received from FNAL. The Hall B Instrumentation Group modified the DAQ hardware and software to run lab and beam tests. Some of the significant modifications that were made were the addition of plots to show the number of hits in each strip, the archiving of selected real-time strip plots, the storage of output data for off-line analysis, the ability to change the clock-base, and the addition of the external trigger mode. For the operation of the stave, low and high voltage control programs were researched, developed, and implemented [15, 16].

R&D activities during FY2004 culminated with the conduction of beam tests [17]. To perform these tests, specialty cables, data buffers, data repeaters, controls and monitoring programs for low and high voltages, DAQ software, off-line analysis software, support structures, and finite element analyses were designed, developed, debugged, and implemented. The significant result of the FY2004 R&D effort was that it provided hands-on experience with several facets of the endeavor to build a reliable state-of-the-art silicon vertex tracker tailored to meet CLAS12 requirements. For FY2005 the R&D plan was to develop a laser test stand

and a PCI-based DAQ board [18]. However, due to budgetary considerations, work was done only on the laser test stand. Additionally, the prototype FPGA-based, PCI-bus-compatible, printed circuit carrier board for the DAQ controller of the SVT was successfully built and tested [19] (see Fig. 35).

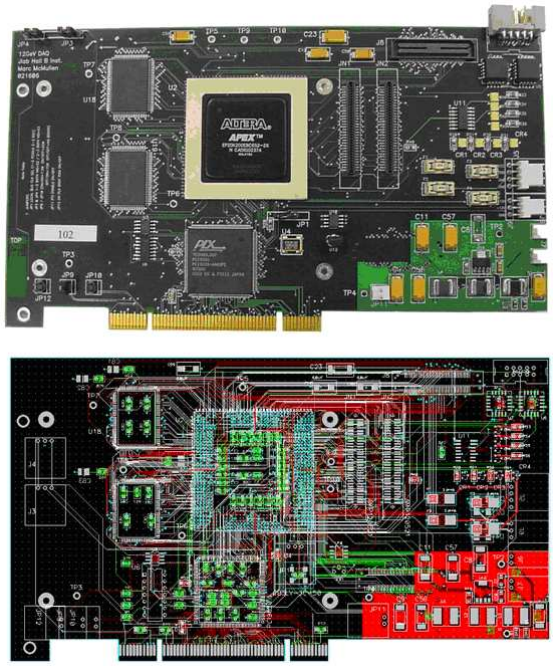

Figure 35: New PCI-based CLAS12 DAQ base board.

R&D for FY2006 focused on the design of the DAQ mezzanine circuit board (shown in Fig. 36) that will be compatible with a VME board. The block diagram for the circuit board is shown in Fig. 37. The FPGA design of the SVT DAQ/controller board is flexible and permits use of different silicon sensor readout ASICs.

R&D on the advanced conceptual design for the SVT is continuing. Support structures and instrumentation strategies are being developed, and detector installation procedures are being studied. Safety issues for each step of the detector construction and installation are being analyzed.

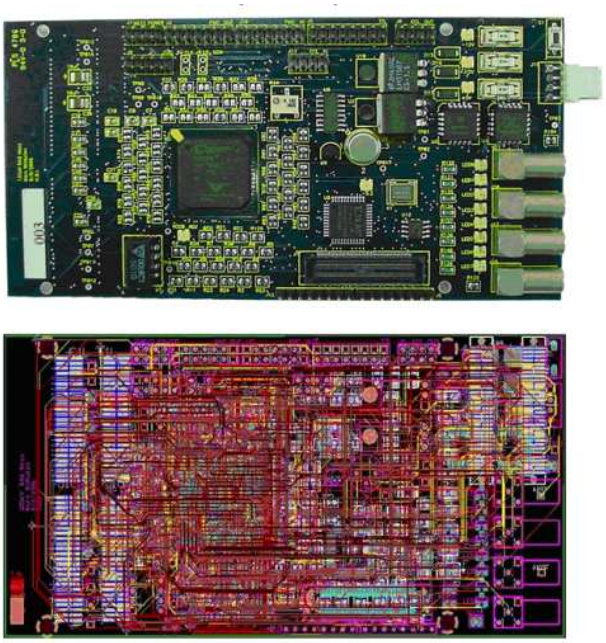

Figure 36: SVX4-based PMC controller card.

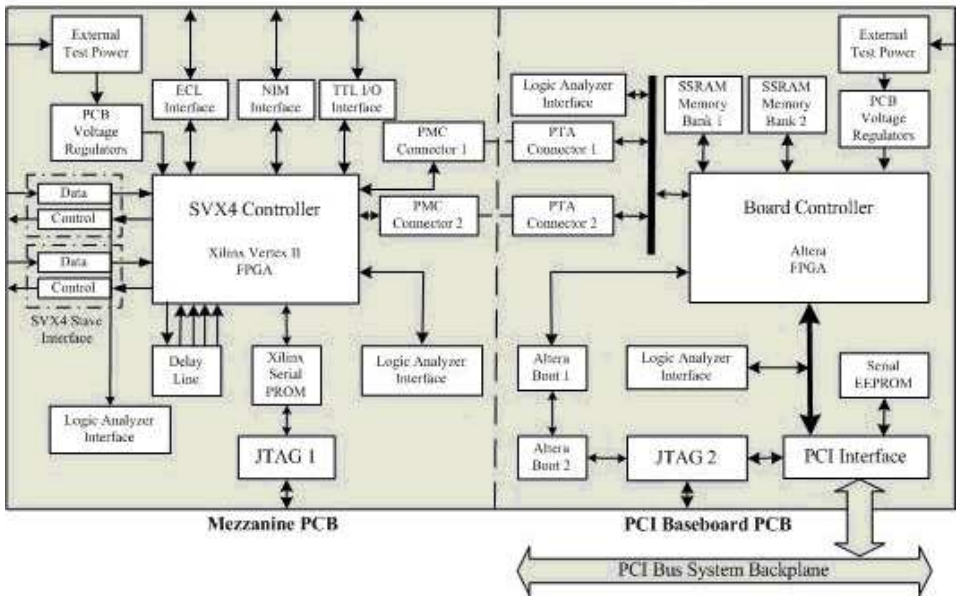

Figure 37: Prototype DAQ circuit board diagram.

7 Expected Tracking System Performance

7.1 Rate Dependence of the Central SVT Tracking

We have studied rate effects in the central SVT (the BST). A GEANT4 study shows that the primary accidental background impinging on the BST is γ rays, and that the total rate will be about 10 MHz per layer. The vast majority (>90%) of these photons produce only one hit in a particular layer. We have conducted two studies of the effect of background on the BST: in one we studied the effect of uncorrelated background while in the second we used a realistic GEANT4 simulation of the electromagnetic and hadronic background.

The first study considered uncorrelated, evenly-distributed background. Because the number of strips per layer is very large, the main deleterious effect of such a background is to produce 'fake' tracks from these accidental hits. We applied a cut-based track-finding algorithm to a set of events generated from random hits in each layer, augmented with a 10% 'punch-through' probability, that is, for each hit, there was a 10% chance that a strip in the adjacent layer would also be hit. We tuned up the cuts so that true tracks were found with greater than 95% probability. Fig. 38 shows the number of reconstructed fake tracks plotted vs. the assumed rate of accidental hits per layer for two cases: one with a 6-layer BST and the other with an 8-layer BST. For each configuration, we see a similar behavior: at low background there are few fake tracks and the number begins to grow exponentially at some background level. Note that these fake tracks can be significantly reduced using other information, e.g. the central TOF counters, but nevertheless, we would like to keep the number of fake tracks as found in the BST alone below some number, for example, five per event. Fig. 38 shows that if we wish to stay below five fake tracks per event, an 8-layer BST design will extend the luminosity reach of the detector by about 40% over a 6-layer design. We also note that a 10-MHz accidental background integrated over the 150-ns live-time of the SVT will create only about 1.5 accidental hits per plane. At this level of background, we should find essentially no fake tracks and the accidental background will be dominated by real, out-of-time hadrons from other events.

The second study was a full GEANT4 simulation followed by realistic event reconstruction in the presence of the background. After optimizing our reconstruction code on clean events, we turned it to the task of finding one (known) track embedded in a sea of background. As expected from the simpler study, we saw very little loss of efficiency in finding the known track,

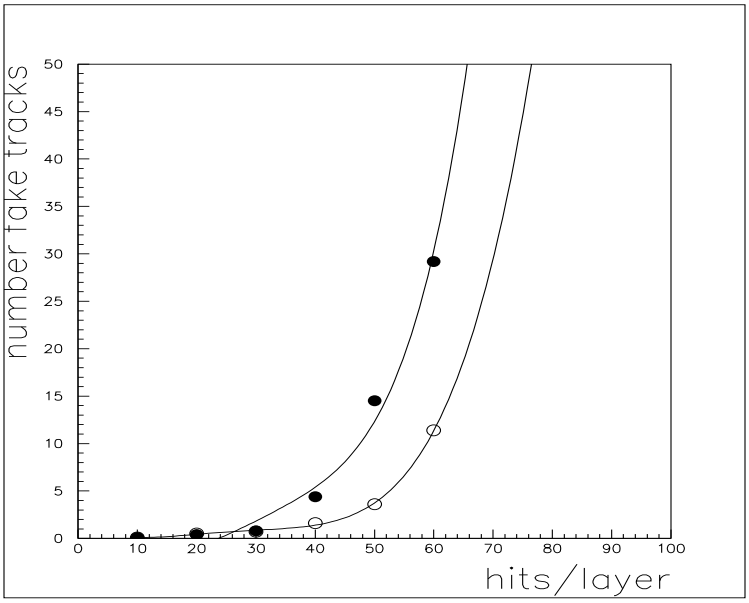

Figure 38: A plot of the number of reconstructed fake tracks as a function of the number of accidental hits per layer in the BST for two cases: a 6-layer (filled) and an 8-layer (open circles) version.

but we did find accidental tracks. The number of these accidental tracks was proportional to the background rate and had a characteristic shape. If there was a real track in the simulated event, then the background consisted of two parts:a number of "sister" tracks with nearly the same momentum as the real track and a smooth background of fake tracks with no connection to the real track. This smooth component peaks at small values of momenta. The "sister" tracks are caused by using most of the hits from the real track along with the wrong choice of hit, when an accidental hit was adjacent or very near a real hit. These combinations would probably be removed during an analysis, but they will worsen the resolution.

Our studies also show that the number of fake tracks is very sensitive to a cut on the energy deposited in a single strip. It seems that we can remove most of the fake track candidates with a 20 KeV cut on the hits from the BST. Note that a minimum ionizing particle is expected to deposit about 140 KeV of energy on traversing one strip.

7.2 Rate Dependence of the Chamber Tracking Efficiency

As discussed above, the `CLAS12` detector is designed to detect semi-inclusive and exclusive events with a modest number (up to 4 or 5) of outgoing hadrons. In addition to the electron and hadrons associated with the event of interest, the detected event will contain both electromagnetic and hadronic "accidentals". Because the physics goal is to run at beam-target

luminosities of 10^{35} cm^{-2}s^{-1} or higher, we have simulated the expected accidental particle flux associated with these luminosities. Using a modified version of the EGS program [20], we simulated the total hadronic and electromagnetic particle fluxes generated when an electron beam is incident upon a liquid-hydrogen target with a luminosity of 10^{35} cm^{-2}s^{-1}. We calculated the total flux through a measurement layer during its active (measurement) time and multiplied by the probability of the particle interacting in that layer and divided by the number of cells in the layer to get an estimate of the fractional occupancy of that layer due to background. Our GEANT3-based model of `CLAS12` includes the current design of the tracking detectors, the magnetic field from the torus and solenoid, and the key absorbers to simulate background during an event. We combine this background event with a simulated single-particle track through the chambers, and run our normal track reconstruction code on the combined event.

The expected layer occupancy for all drift chambers under these conditions is below $\sim$2% as shown in Fig. 39. Our experience with the present `CLAS` detector is that track-finding is highly efficient if the accidental occupancy is less than 4% [21]. Fig. 40 shows the efficiency of our present tracking program for finding a track as a function of the fractional occupancy of Region 1, that is, the percentage of wires that fired for the event in question. One can see that the efficiency begins to fall off at a fractional occupancy of about 4%. Finally, Fig. 41 shows the tracking efficiency as a function of luminosity. Our studies indicate that even at luminosities up to $\sim 5\times10^{35}$ cm^{-2}s^{-1}, the tracking efficiency remains at or above the 95% level.

Our GEANT3 rate simulations indicate that the number of accidental tracks (not associated with the event in question) crossing the Region 1 drift chambers during their sensitive time at a luminosity of 10^{35} cm^{-2}s^{-1} is significantly less than that simulated for a recent experiment, E1-DVCS, which employed a similar solenoidal shield for Møller electrons and which ran at a luminosity of 2×10^{34} cm^{-2}s^{-1}. We are continuing to run more detailed simulations to verify this result.

7.3 Charged Track Resolution

We have used two methods to simulate the expected momentum, angle, and vertex resolutions for the `CLAS12` tracking system. In one, we use the MOMRES [22] program to estimate the resolutions in the bend plane and a simple linear fit to estimate the resolutions in the non-bend plane. The second method is to use the full power of a GEANT3 simulation and full track

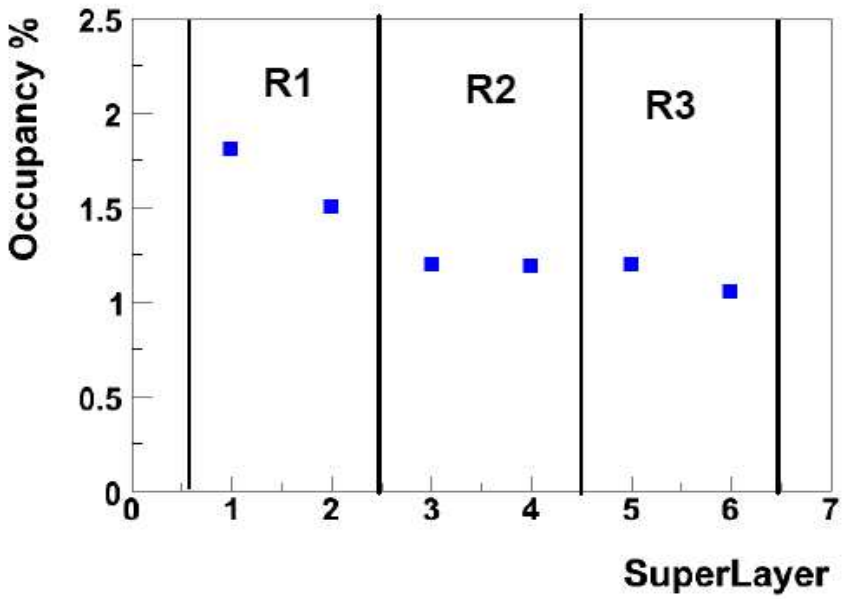

Figure 39: Plot of drift chamber occupancy vs. superlayer number at a luminosity of 1×10^{35} cm^{-2}s^{-1} showing the fall-off with increasing r. The data were simulated using GEANT3. The vertical lines mark the boundaries of the Region 1, 2, and 3 drift chambers.

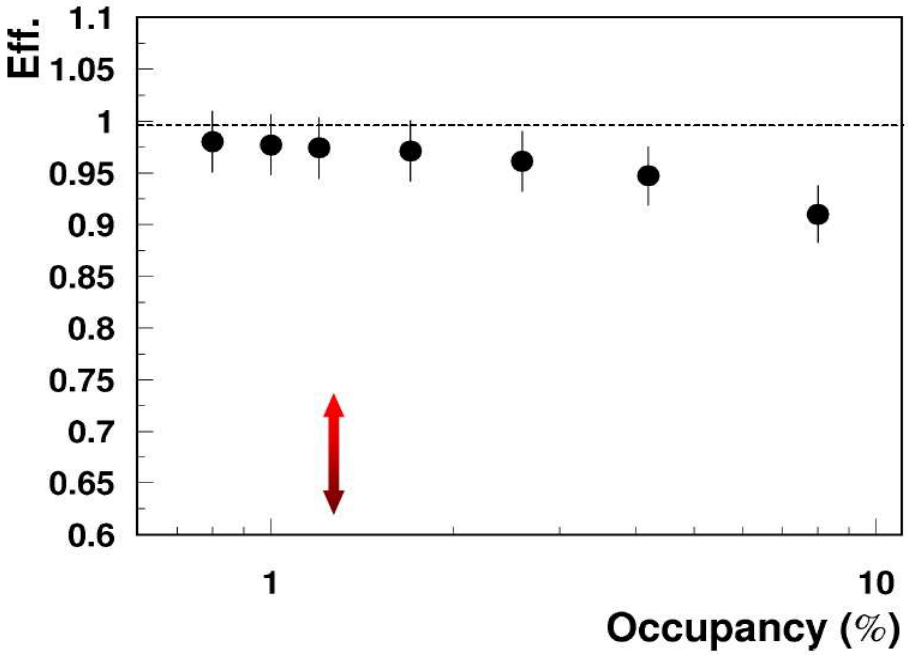

Figure 40: Plot of tracking efficiency vs. the fractional number of wires with hits in Region 1. The data were simulated using GEANT3. The arrow indicates the expected occupancy at a luminosity of 1×10^{35} cm^{-2}s^{-1}.

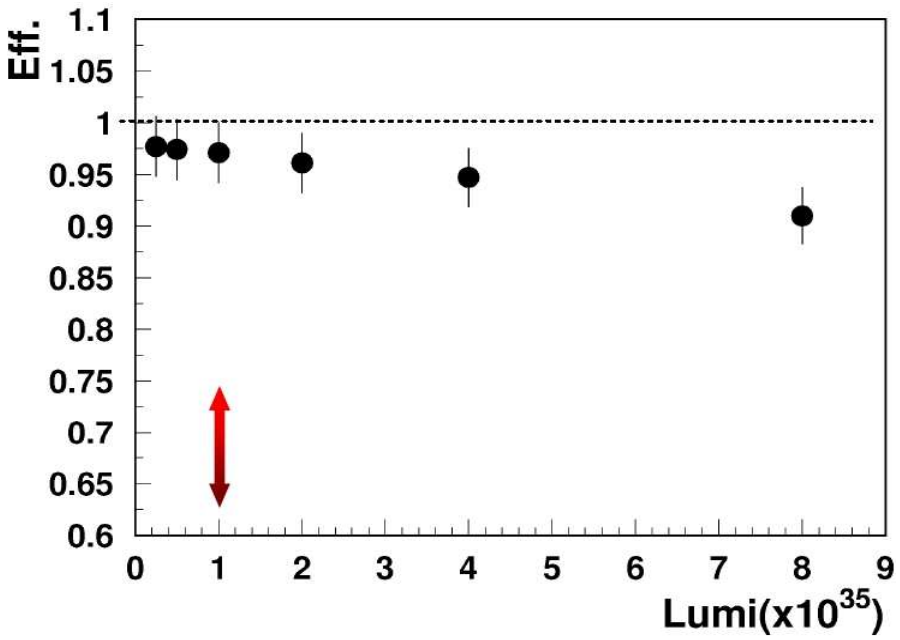

Figure 41: Plot of tracking efficiency vs. luminosity showing the fall-off with increasing rates (and hence occupancy). The data were simulated using GEANT3.

reconstruction to estimate the resolution on the track parameters simultaneously.

We studied the position, angle, and momentum resolution for a number of possible detector options using MOMRES. The input file to MOMRES characterized the detector position, material thickness, and estimated hit resolution for a particular track angle. We also produced a B-field file that was a tabulation of the B-field strength (for the torus and central solenoid) vs. path length for a particular track angle. These, and the desired range of momenta, were then used to calculate the expected components of the resolutions due to multiple scattering and measurement resolution. We fit these outputs to the expected kinematic form. From these fits we extracted two parameters (σ_1 and σ_2) for each of the three terms (dp/p, $d\theta$, dx). These six parameters summarize the output of MOMRES. In addition, we calculated the angle resolution in the non-bend plane in a manner analogous to that of MOMRES, using estimates for the effects of multiple scattering and measurement error, fitting the resulting smeared trajectory by a straight line, and extracting the σ_1 and σ_2 parameters that characterize the resolution in the non-bend plane angle. Thus, eight parameters for each value of track angle fully characterize the tracking resolution for any one detector option. Fig. 42 shows the momentum resolution for tracks emitted at various angles as a function of momentum.

Fig. 43 shows comparisons of the momentum resolution plotted vs. momentum for three different conditions. One is for a MOMRES calculation of our standard set-up, with 6 layers

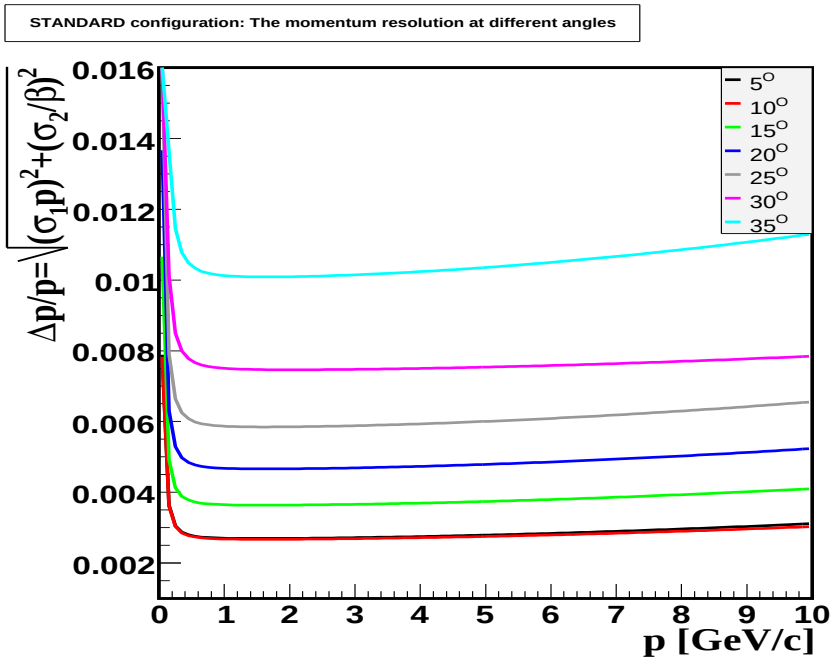

Figure 42: Resolution simulated using MOMRES plotted vs. particle momentum for tracks emitted at various forward angles from 5° to 35°. The momentum resolution is better at smaller angles because the traversed integral magnetic field is higher.

of a Forward Silicon Tracker (FST) followed by our three regions of drift chambers; the second is for the same setup but without the FST. Finally, the third curve shows the result of increasing the spatial resolution of the drift chambers from 250 to 350 μm. Note that our standard case, with the FST, has better resolution at higher momentum because of the extra measurement points from the FST, but has worse resolution at low momenta, because of the additional multiple scattering of the six layers of the FST. Fig. 43 also shows the three cases for the angular resolution vs. momentum; there is not much difference between them. Finally, Fig. 43 shows the dramatic improvement in vertex resolution provided by including the FST information.

Fig. 44 provides a few more results of these MOMRES studies to parameterize and understand the resolution expected for the `CLAS12` tracking system. The plots show the expected angular resolution and position resolution for different angle bins, each as a function of momentum. These plots were made using the current design of the tracking system. Finally, Figs. 45 and 46 are included to show the complete agreement between the results of our MOMRES calculations of the resolution and our full GEANT3 simulations.

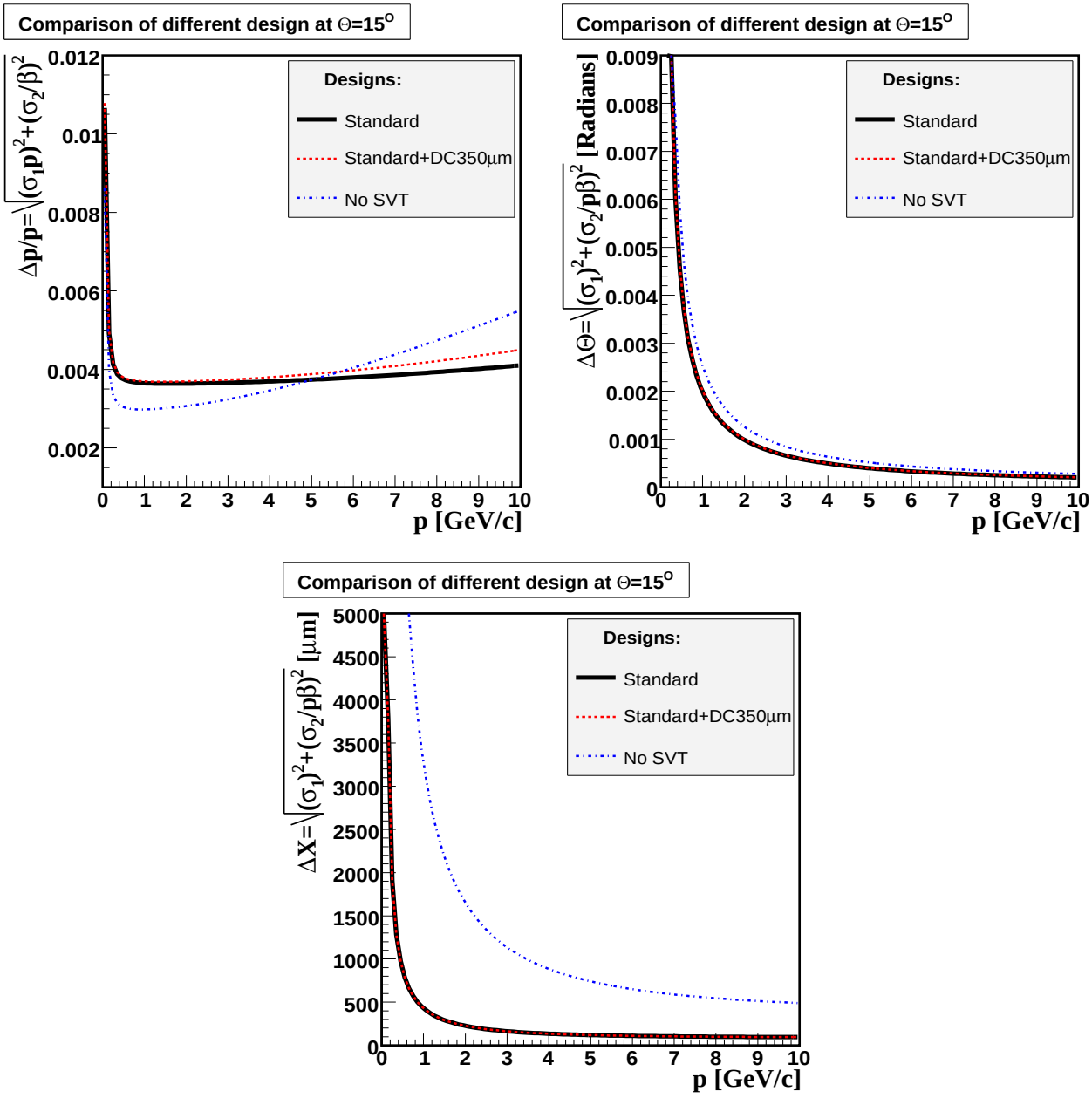

Figure 43: Momentum resolution (top left), θ resolution (top right), and impact parameter resolution (bottom) simulated using MOMRES for 3 different conditions (see text for details) plotted vs. particle momentum for charged tracks emitted at 15°.

Finally, Figs. 45 and 46 are included to show the complete agreement between the results of our MOMRES calculations of the resolution and our full GEANT3 simulations.

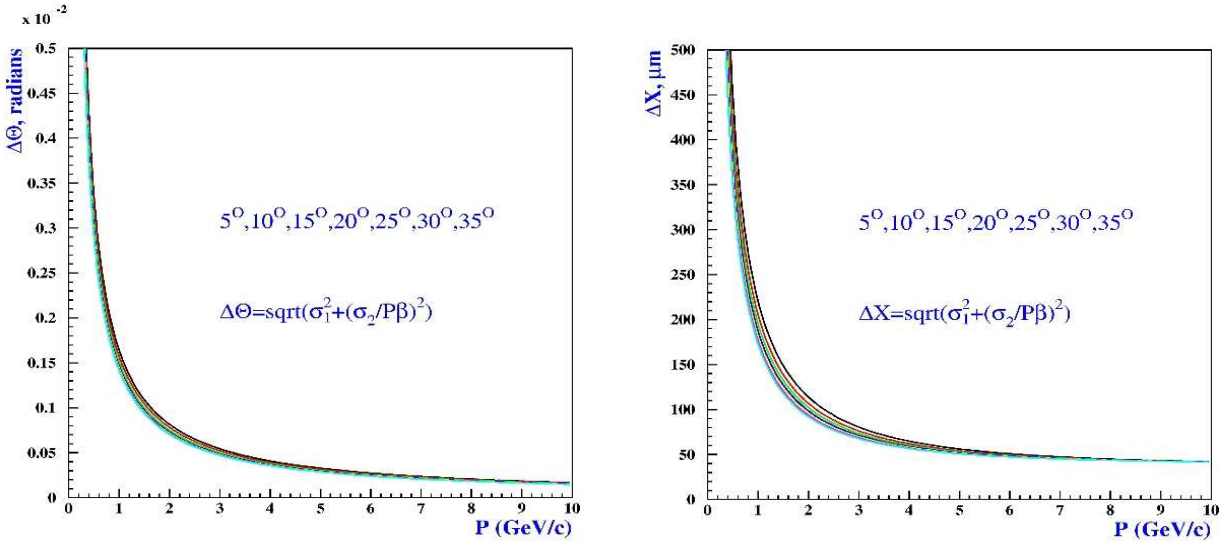

Figure 44: Simulation results for the CLAS12 tracking system using MOMRES showing the expected angular resolution and position resolution for different angle bins as a function of momentum.

7.4 Charged Track Resolution in the Barrel Silicon Tracker

Tracks with polar angles greater than 35° are reconstructed in the BST alone. As in the case for forward-going tracks, we have used two methods to simulate the expected momentum, angle, and vertex resolution. In one, we use the MOMRES [22] program to estimate the resolutions in the bend plane. The second method is to use the full power of a GEANT4 simulation and full track reconstruction to estimate the resolution on the track parameters simultaneously.

As mentioned in the design section the Silicon sensors have strips angled at a stereo angle. To provide maximum acceptance, the strip stereo angle is not constant but varies continuously from 0° to 3° on each sensor. This results in an average crossing angle between neighboring planes of approximately 2.5°. The strip pitch also increases with z because of this graded layout. The longer the z-coverage of a particular layer, the greater the strip widens. The result is that the average strip pitch varies from 160 to 190 microns as one goes from layer 1 to layer 4. These parameters are all taken into account in our simulation.

In Fig. 47 we show our expected resolutions for momentum, θ, ϕ and z for 60° tracks as a function of momentum. The full GEANT4 simulations and reconstructions are shown as the

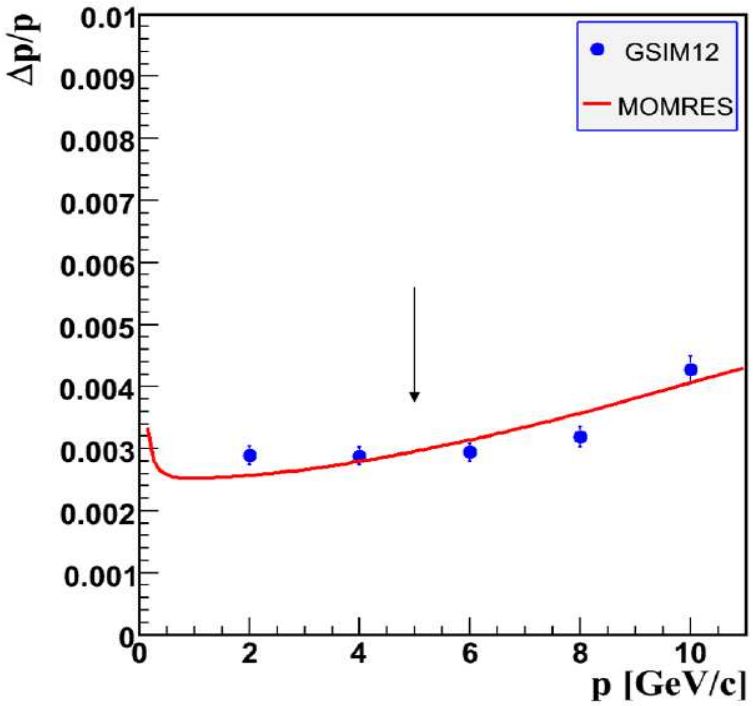

Figure 45: Comparison of momentum resolution of CLAS12 vs. momentum. The curve is from our calculations using MOMRES and the data points are from our GEANT3 simulations of CLAS12 (called GSIM12).

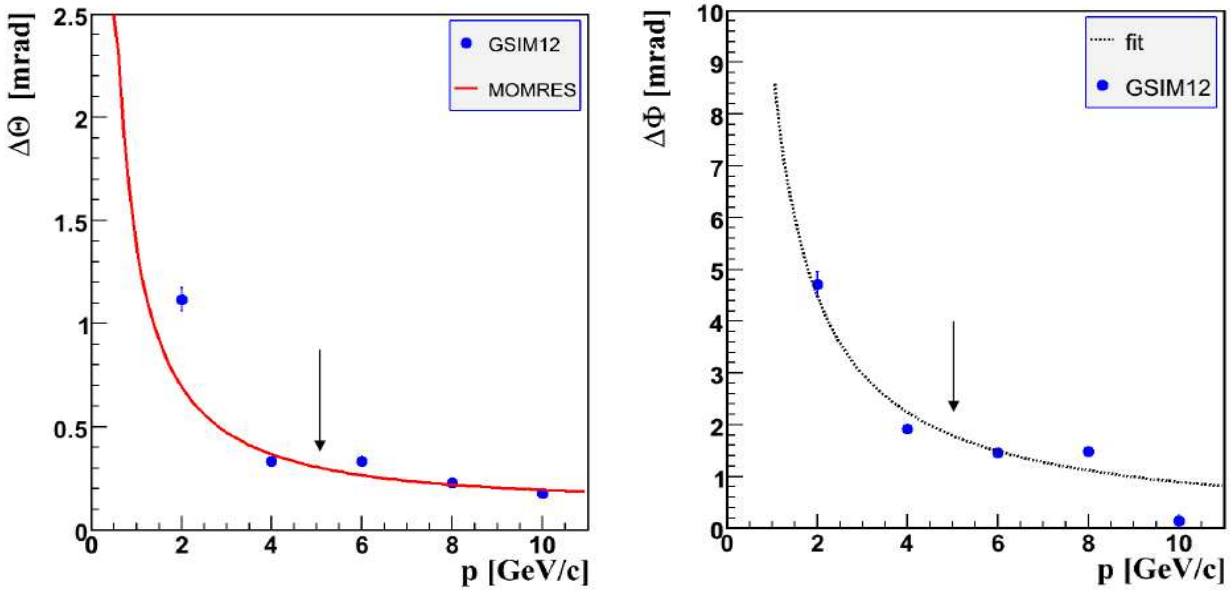

Figure 46: Comparison of θ and ϕ angular resolution of CLAS12 vs. momentum. The curve is from our calculations using MOMRES and the data points are from our GEANT3 simulations of CLAS12 (called GSIM12).

curve, while the simpler MOMRES calculations for momentum and ϕ are shown as the points. Although MOMRES does not capture the full sublety of the detector (for example, it considers that the two alternating strips at different stereo angles are at the same radius) it is consistent with the GEANT4 result. From the figures, one can readily see that the resolutions in (dp/p, $d\phi$ and $d\theta$) of 2.5%, 4 mrad and 17 mrad respectively exceed our general requirements for the resolution of the central tracker.

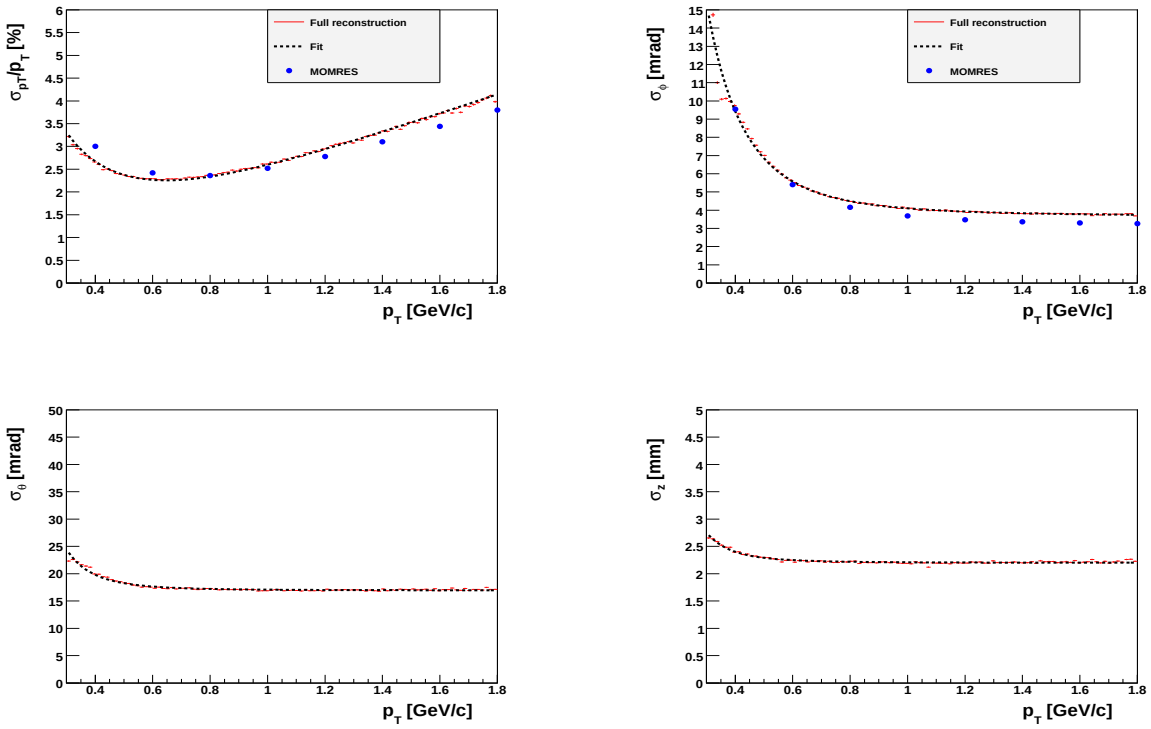

Figure 47: Simulation results for the CLAS12 BST tracking system. Separate plots are shown for momentum (top left), ϕ (top right), θ (bottom left) and z (bottom right). The full GEANT4 simulation results are shown as the curves, while the MOMRES calculations are shown as points.

8 Expected Physics Performance

We have used a series of programs to calculate the acceptance and reconstructed physics parameters for event types of interest. The program CLASEV [23] served as an event generator and analysis program. Depending on the value of input flags, it generates certain types of events, that is, it produces a set of 4-momenta for the primary hadrons in the hadronic center-of-mass and allows some of them to decay into the final-state hadrons and transforms their

momenta to the lab system. For each final-state track, it calls FASTMC (our fast, parametric Monte Carlo program for CLAS12) to determine if the track falls within a fiducial acceptance window and to determine its final, smeared lab momentum. It then produces selected physics analysis variables (e.g. missing mass) from calculations involving the smeared momenta of the tracks that were accepted. Fig. 48 shows the expected missing mass resolution expected for CLAS12 from FASTMC simulation studies based on the current design specifications for a number of different reactions. For all cases studied, the results are quite encouraging in terms of identifying the missing particle cleanly for each reaction. Our GEANT3 results are in accord with the FASTMC results.

We also show some results from our FASTMC simulation of $e\pi^+$ events in which the recoil baryon is detected by missing mass. Fig. 49 shows the missing mass spectrum expected when the π^+ is detected in the forward tracker (left) or central tracker (right). We have sufficient resolution to study resonant production and to compare, for example, u-channel, s-channel and t-channel processes.

9 Safety and Quality Assurance Issues

9.1 Safety

There are safety issues in the construction, installation, and operation phases of the CLAS12 SVT project that we address in this section. Safety will be addressed from the start as an integral part of all activities and plans. All of our workers will receive appropriate training prior to being permitted to perform any activities on the detector.

The only significant safety issues are in the construction, installation, and operation of the SVT. During the construction phase, we receive a number of machined parts from industry that must be cleaned thoroughly before assembly. Our anticipated cleaning strategy is to use safe, non-volatile cleaning agents that are friendly to the environment and to human health. All of our activities are coordinated by written procedures that are reviewed by our EH&S professionals at the lab.

The normal operation also involves delivery of low-voltage power to the on-board amplifiers. Although the low voltage (less than 8 V) means that there is no electrocution hazard, there is a potential for over-heating and fire ignition because of the currents involved. The

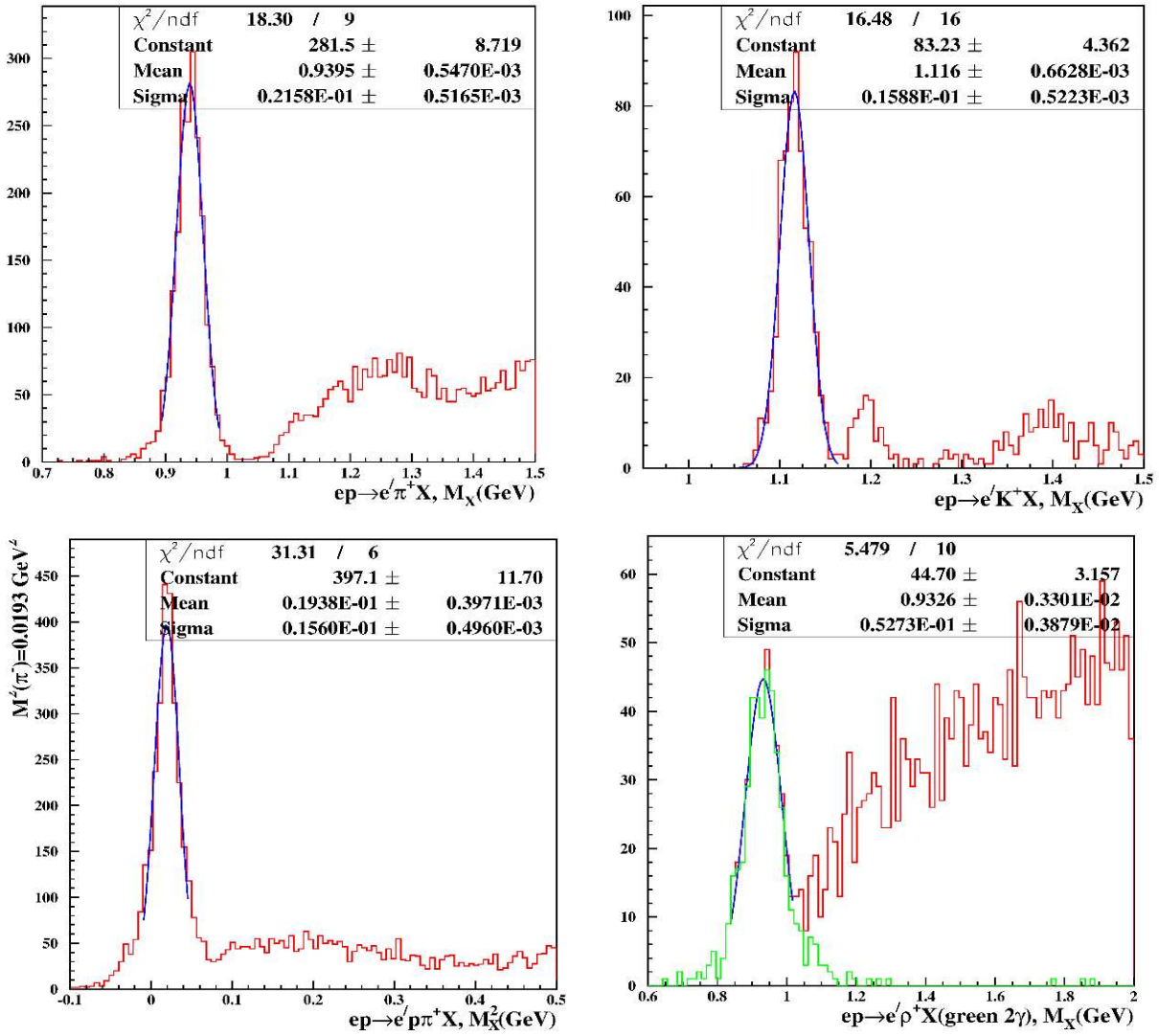

Figure 48: Simulation results from FASTMC highlighting the expected missing mass resolution of CLAS12 with the nominal design specifications for the tracking detectors (drift chambers and SVT). Shown are the spectra for the reactions $ep \to e'\pi + X$ (UL), $ep \to e'K^+X$ (UR), $ep \to e'p\pi^+X$ (LL), and $ep \to e\rho^+X$ (LR).

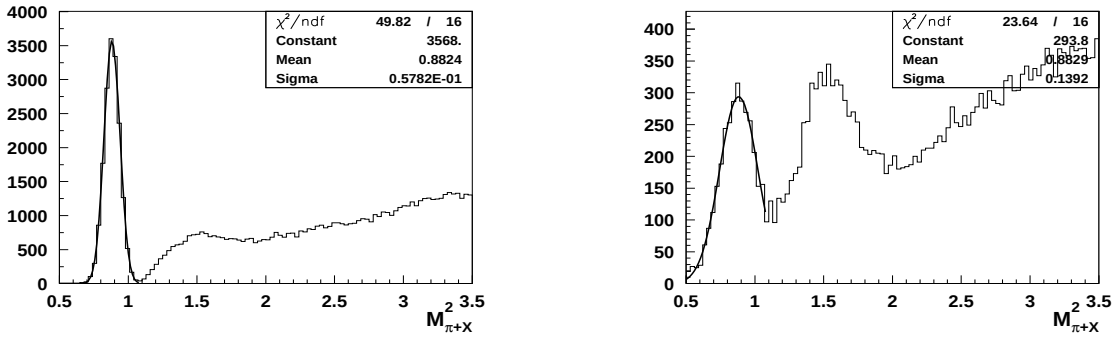

Figure 49: Simulation results from FASTMC highlighting the expected missing mass resolution of CLAS12 for events in which we detect only a π^+ and the electron for two cases: on the left when the π^+ is detected in the forward tracker, and on the right when detected in the central tracker.

design of the low voltage system will include appropriate current fusing to ensure safety to personnel and to the equipment.

Operation of the SVT also involves the delivery of high-voltage to the detector. The design of the high voltage supplies will include over-current and over-voltage protection. Administrative procedures are in place to prevent accidental shocks from taking place.

9.2 Quality Assurance

Quality Assurance (QA) begins before the procurement of components and detector construction and continues beyond detector installation and commissioning. This section details plans for QA for the SVT for CLAS12.

QA planning for the SVT system includes the following areas:

- Bench testing of each of the individual components of the SVT hardware prior to module assembly. This includes the silicon sensors, readout chips, circuit boards, wire bonds, and cabling;
- Testing of complete stave assemblies and modules prior to assembling the detector as a unit;
- Encapsulation of the wire bonds to prevent breakage or stress;
- Including fiducial marks on all custom silicon components for alignment;

- All assembly will be done in a class 1000 clean room following established clean room conventions;
- Use of custom fixtures to prevent damage during shipment of components;
- Use of alignment markers on the support structure for detector installation.

The quality assurance planning is being done in conjunction with a value engineering (VE) approach for the design. It is expected that the VE for the SVT will improve the QA rating for the design. The steps that are being taken include:

- Use of one silicon sensor size for the barrel SVT and two designs for the forward SVT for a total of only three total different sensor sizes in the system. This allows for a lower number of spares to be purchased and also allows for the possibility that sensor blocks can be interchanged between regions;
- The SVT design employs previously designed readout chips. The design of these chips has therefore been extensively studied and detailed performance evaluations have been completed;
- Common circuit boards and electronic components will be used for the barrel and forward SVT. These boards will follow industry and JLab standards for design;
- Whenever possible, the SVT design makes use of "off-the-shelf" components to improve reliability.

9.3 Conformance with JLab ES&H Manual

All activities will be analyzed in accordance with the JLAB ES&H Manual to identify any and all hazards associated with the work and any and all safety requirements mandated. All persons involved and all persons in the vicinity will be briefed on all potential hazards involved in all activities. However, all activities are considered low risk, common, and routine in nature and are all fully covered by the ES&H Manual.

Many operations will be performed around and in the vicinity of equipment and other activities. Procedures to identify and mitigate risks due to trip and fall hazards will be developed. Similar procedures will be developed for work involving the use ladders, work

platforms, and scaffolds. Standard safety procedures will be followed for all work involving the use of cranes and hoists. Instrumenting, testing, and troubleshooting the detectors may require Class 1 Mode 1 and Class 1 Mode 2 limited testing and diagnostics and will be performed according to EH&S requirements.

10 Collaboration

At present, the SVT collaboration consists of the following institutions:

- Moscow State University, Moscow, Russia
- State Scientific Center of the Russian Federation-Institute for Theoretical and Experimental Physics, Moscow, Russia
- University of New Hampshire, USA
- University of Connecticut, USA
- Institut de Physique Theoretique CEA/Saclay, Gif-sur-Yvette, France

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