Road to SiD Test beam at LNF (Frascati) BTF
23 – 30 June.

22 June DEAD LINE

March: Set-up the DAQ acquisition system.

April: design and assembly the frame for the SID.

Work on **SID Patch Board** (if they are ready)

12-30 May: Last usefull period for wire-bonding SiD over the PCB

(without Patch)

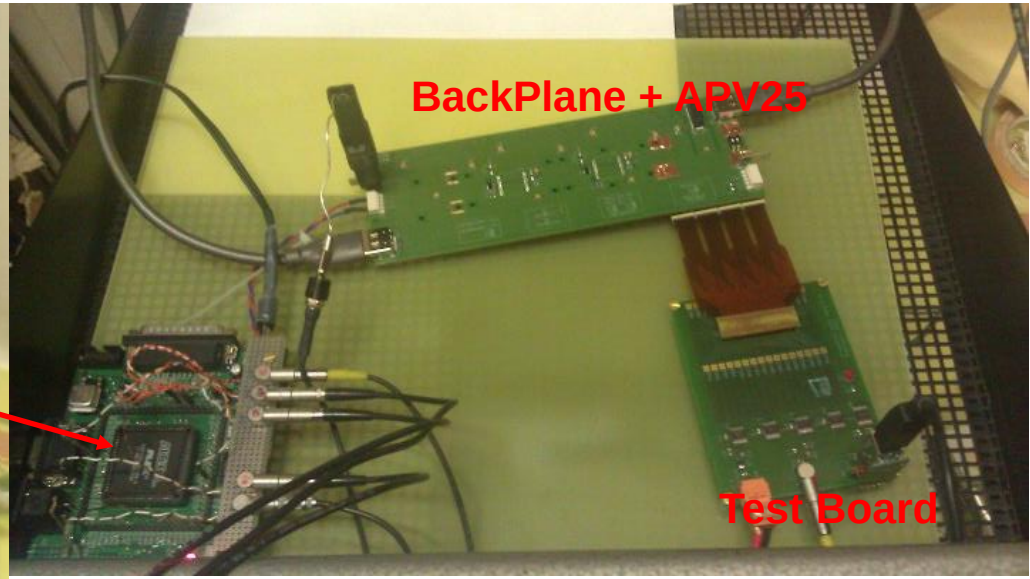
June: Assembly of electronics parts over the PCB

(APV25 connector, BIAS circuit etc)

TEST BEAM (23-29 June)

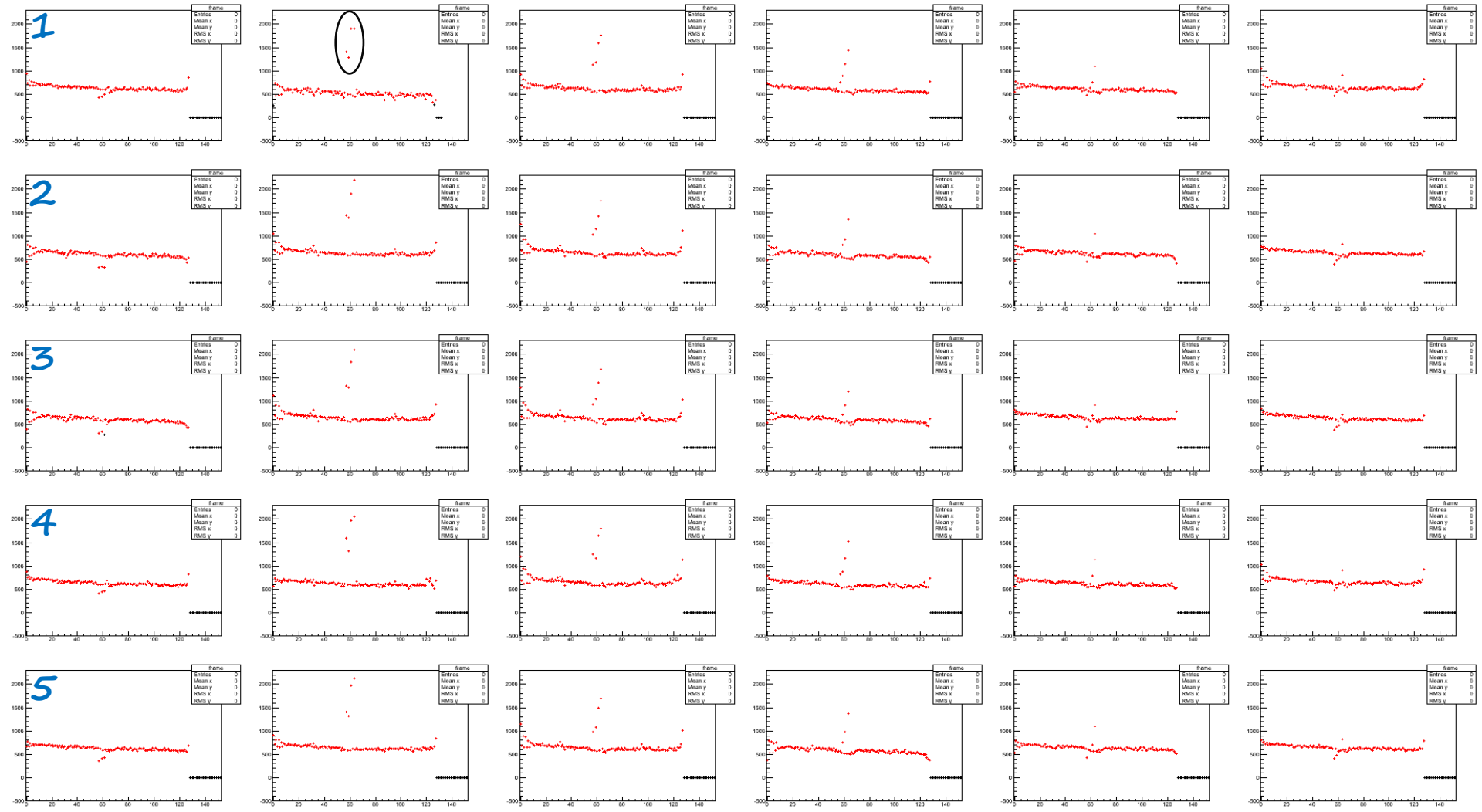
Energy Range e^-	**500 MeV**
Max. Repetition Rate	**50 Hz**
Particles/Pulse	**1**

DAQ Sistem



Upgrade :
From Stand-Alone FPGA
to a VME FPGA

APV25 Response at 1 pulse MIP



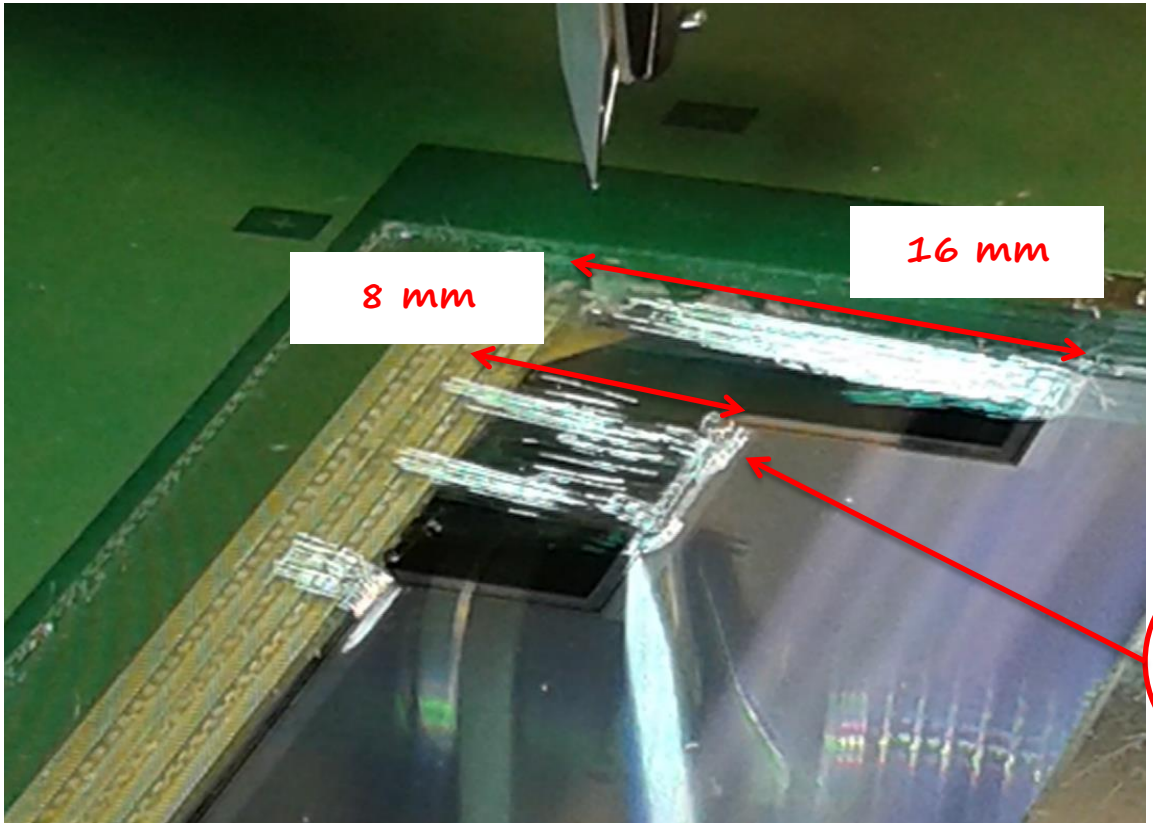
25 APV25 boards to Test (we need 20 APV25 board for the test in June)
Test cables, connection, backplane and adaptors.

Frame for SiD

Customizable Bosch Aluminum Rail for the SiD frame (Prototype)

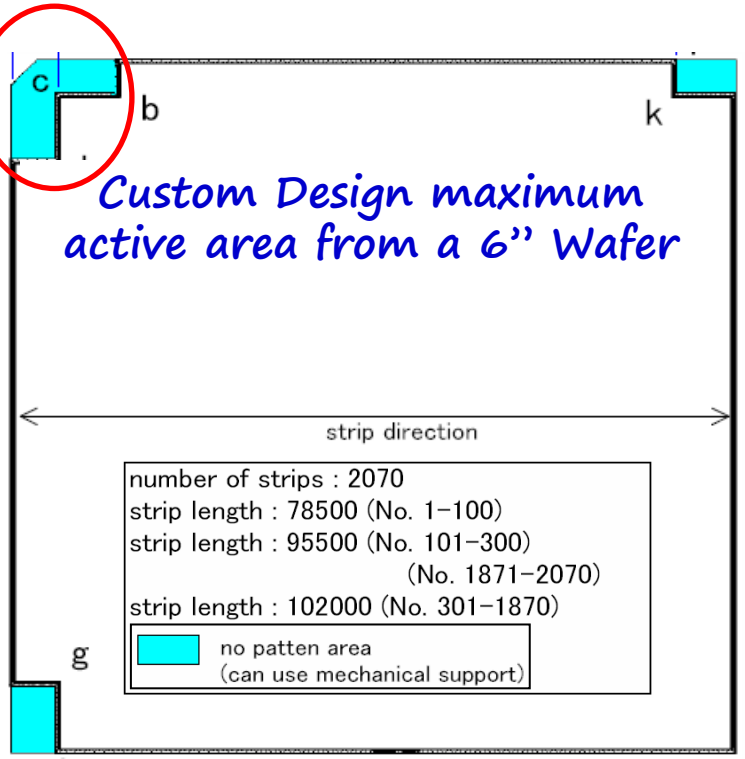
Silicon Patch Board

Possible Problems

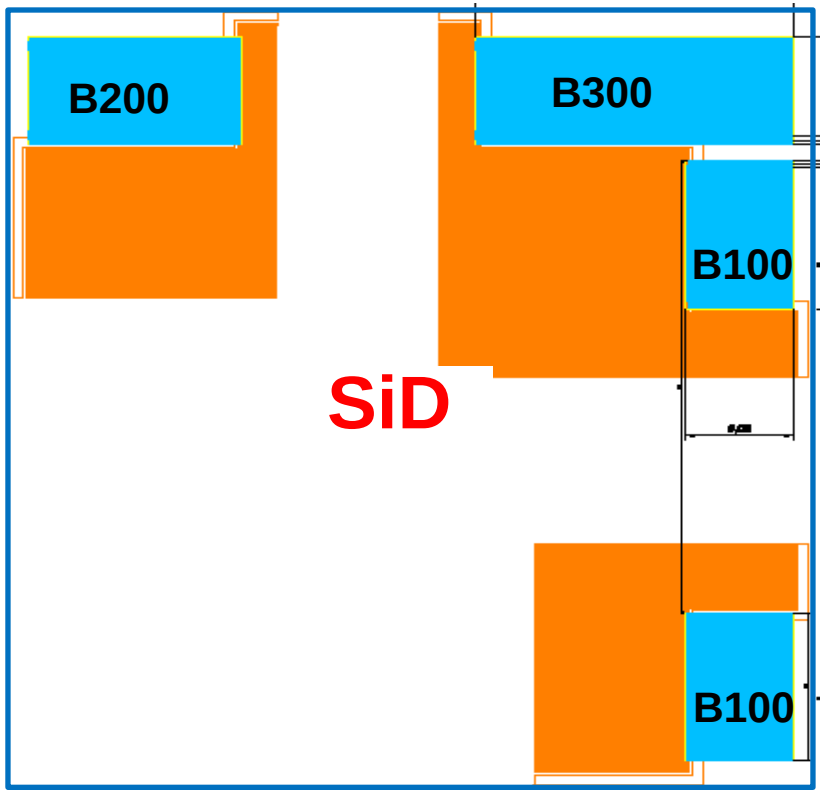


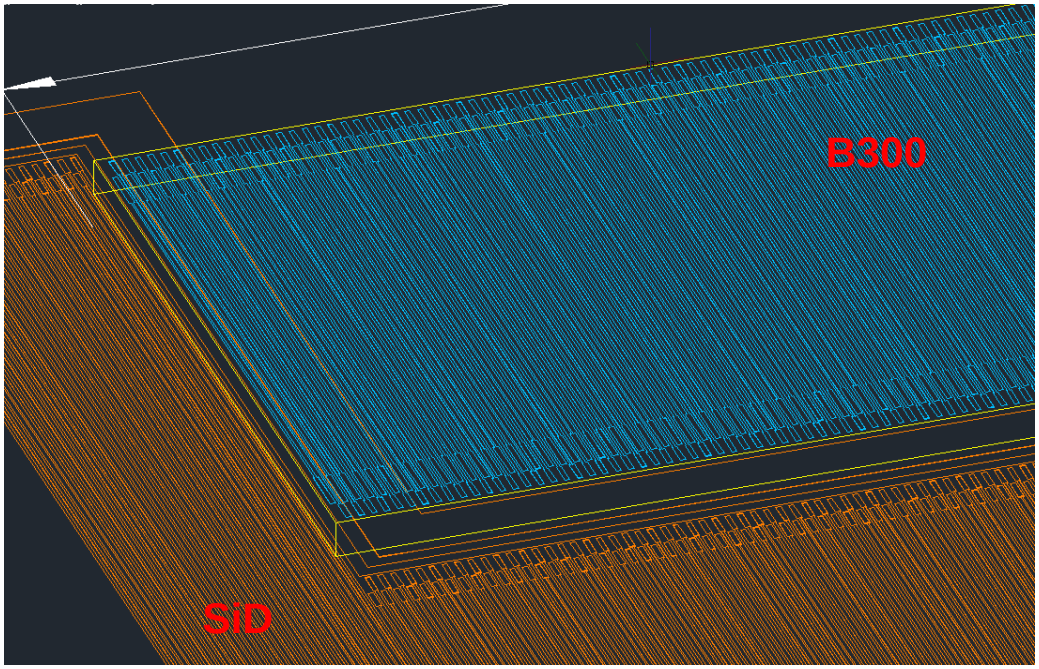
Short Bonding ≈ 4 mm OK!

Long Bonding ≈ 8 – 16 mm
(Problems: possible wire collapsing, wire tilts, with shorts as a consequence)



Silicon Patch Board design





Specific:

300 µm thickness

50 µm pitch (as SiD)

Made by **FBK foundry** (Trento, Italy)

Mask Design is already done

Arrival time: May

Assembly

Improvements:

Improved planarity of PCB

Improved stability of the SiD holder during the wire bonding.

Assembly time:

3 weeks for glue SiD on the PCB and the wire bonging of the SiD strips. (May)

Add the Polarization circuit and test SiD polarizazion. (early June)

Assembley of male connector for connect PCB and APV25 boards. (mid June)

Everything has to be ready for the 22 June!!!!!