SuperBigbite DAQ and Trigger electronics

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SBS Review

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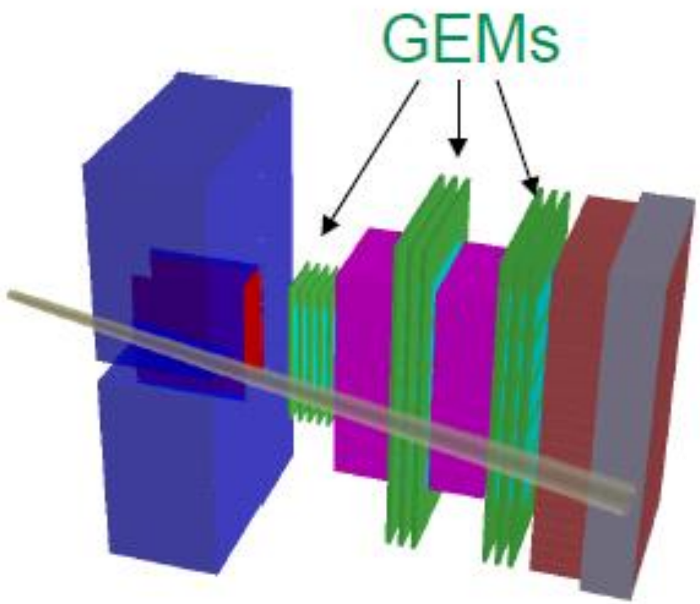
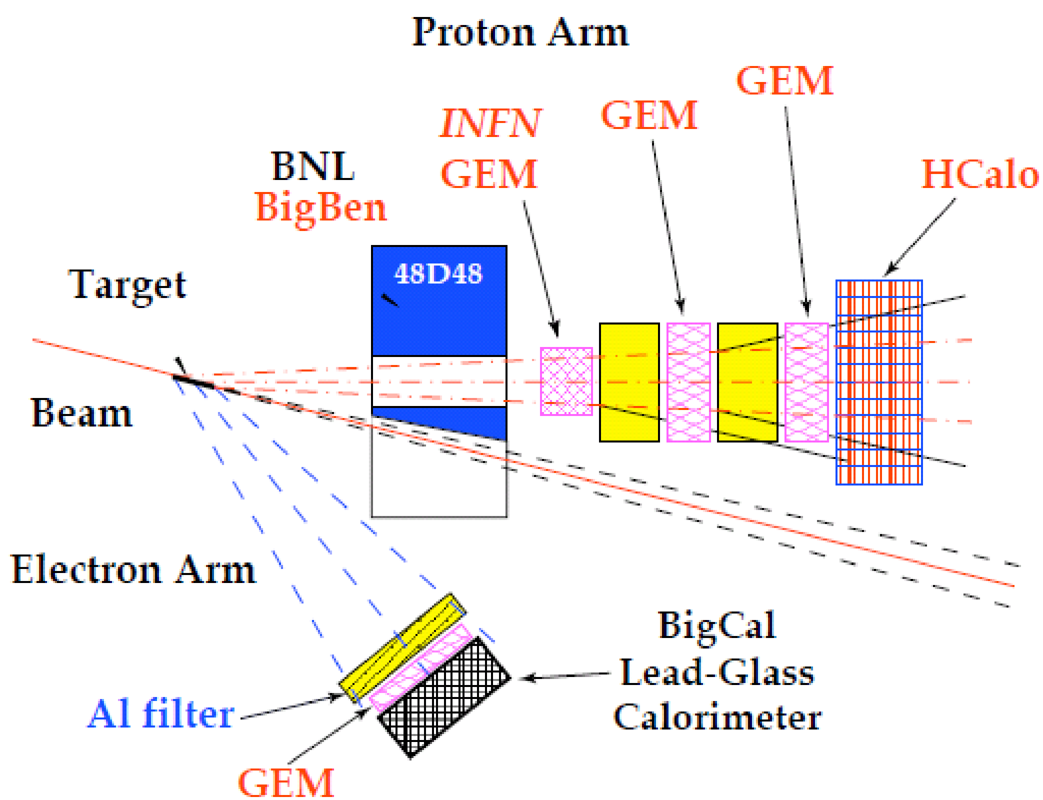
Outline

- SuperBigbite Spectrometer
- Experimental rates
- Trigger and DAQ
- Front End
- Hall A DAQ infrastructure
- Budget / Manpower
- Timeline
- Conclusion

SuperBigbite Spectrometer Focal Plane Polarimeter setup



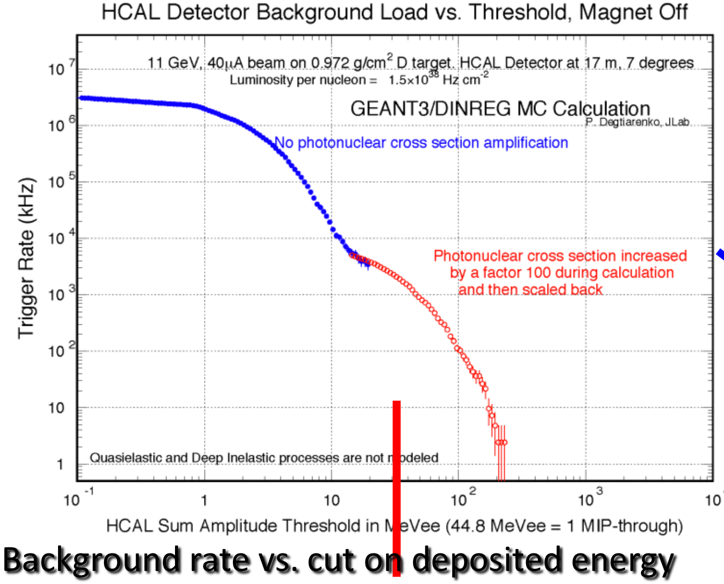


Calorimeter Rates

(CDR section 5.1.7) Most demanding

HCAL

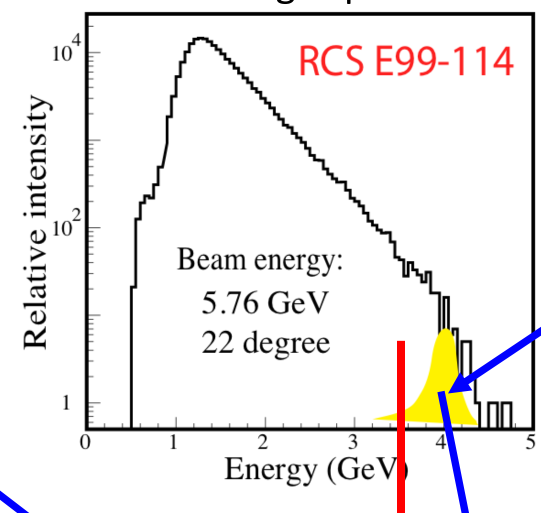
Hadron rate estimate using SLAC & DESY data, Wiser code:
w/4.5 GeV threshold: ≈ 1.5 MHz



Background rate vs. cut on deposited energy (MC studies in progress)

ECAL

From Hall A Real Compton Scattering experiment



NB: Good resolution ≈ 16%/$\sqrt{E}$

Electron rate estimate w/2.5 GeV threshold (73% of E_{elas}): ≈ 200 kHz

≈ 9 kHz coincidence rate w/ 30 ns window

DAQ concept

- Hybrid Fastbus and pipelined electronics
- Level 1
  - ≈100 ns latency by analog summing and discrimination
  - Generated by electron arm (≈200 kHz rate)
  - Gate for Fastbus & non-pipelined VME for BigCal
- Level 2 : coincidence proton in HCAL and electron in ECAL
  - Assume up to ≈1.8 μs latency (L2 800 ns max + Fast Clear 1 μs)
  - 9 KHz with 30 ns coincidence windows
  - FPGA-based coincidence logic using geometrical constraints reduction by factor 5

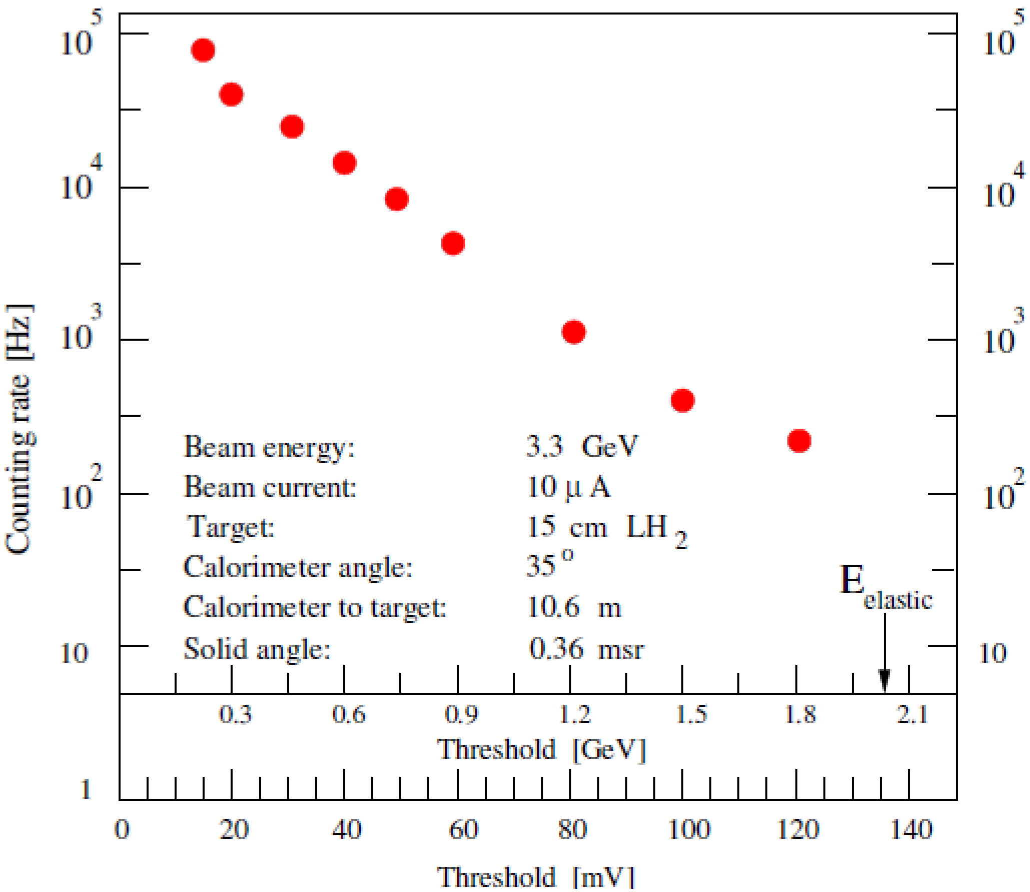
≈ 2 kHz physics DAQ rate

  - Fast Clear FB & VME after L2 timeout ⇒ ≈ 13% Electronics Dead Time

Trigger electronics

- High thresholds to reduce background rate
- Resolution needed at trigger level
  - Summing on electron arm with analog summing for fast trigger in ≈ 100 ns
  - Summing on hadron arm using Flash ADC and FPGA logic for summing and geometrical matching

Electromagnetic calorimeter BigCal readout

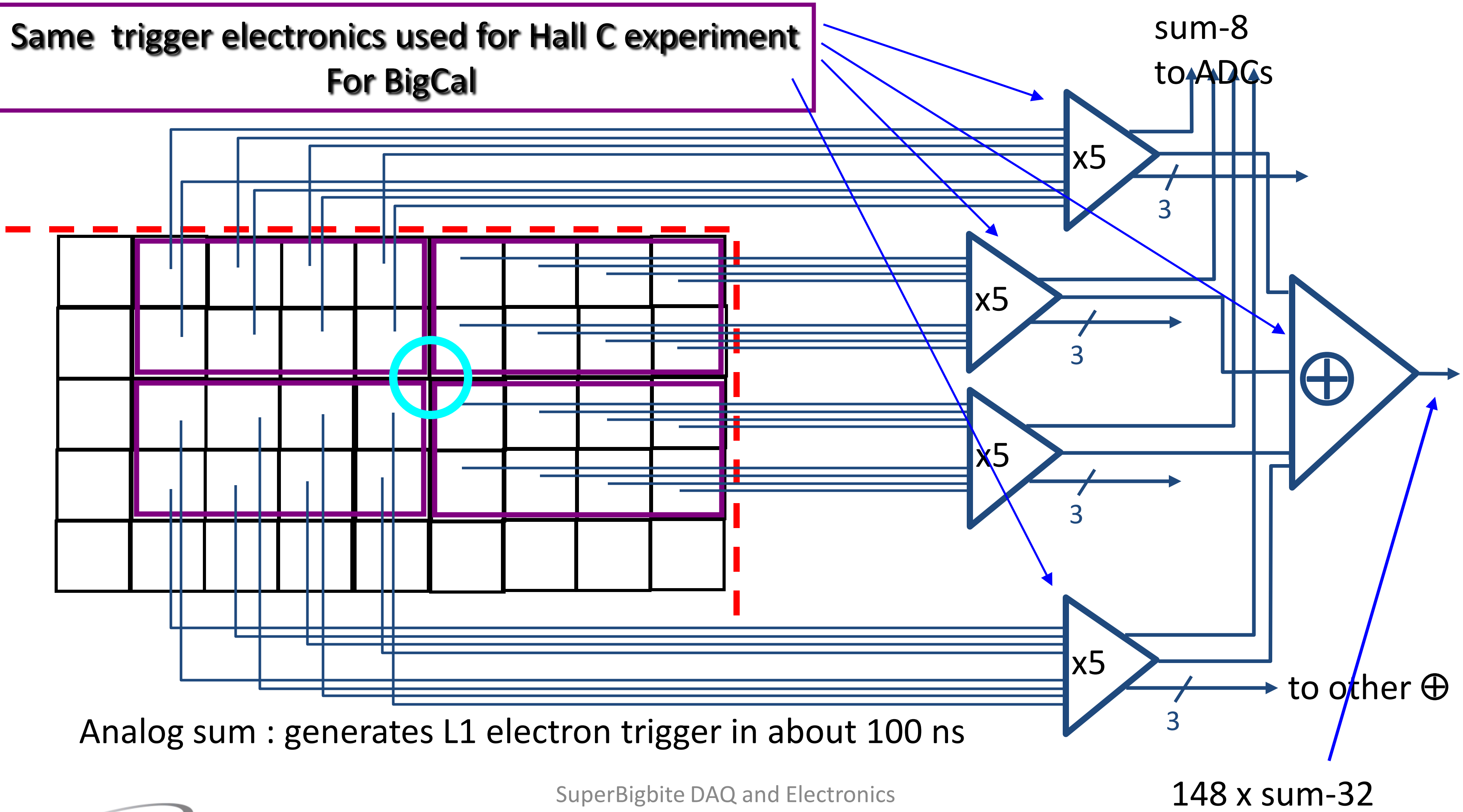


E_{thr}/E_{max} %	50	73	85	90
Rate, kHz	1400	203	60	38

2.5 sigma cut
Calorimeter BigCal resolution
16 %/sqrt E

Electron Big Cal trigger

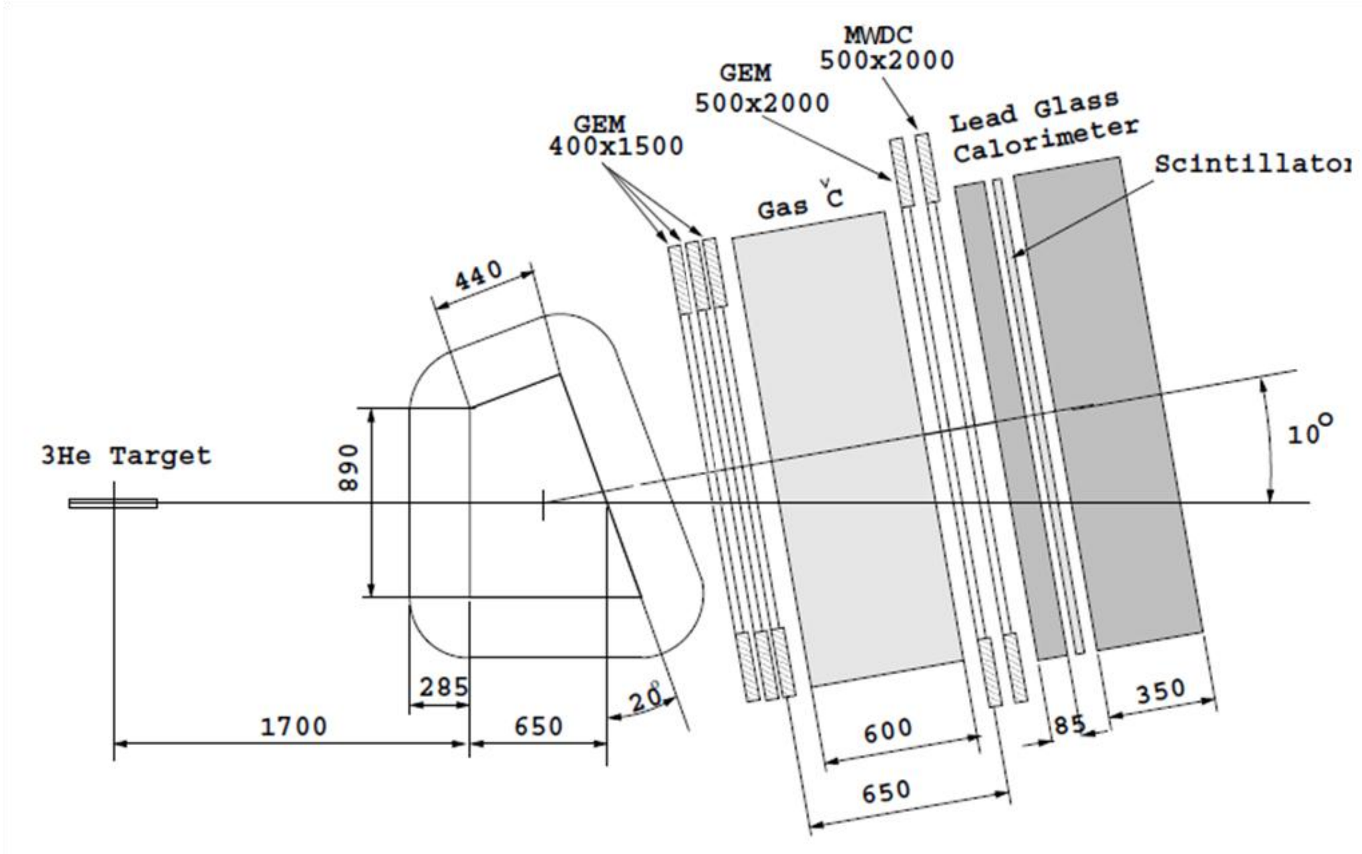
Same trigger electronics used for Hall C experiment For BigCal



Analog sum : generates L1 electron trigger in about 100 ns

Bigbite spectrometer

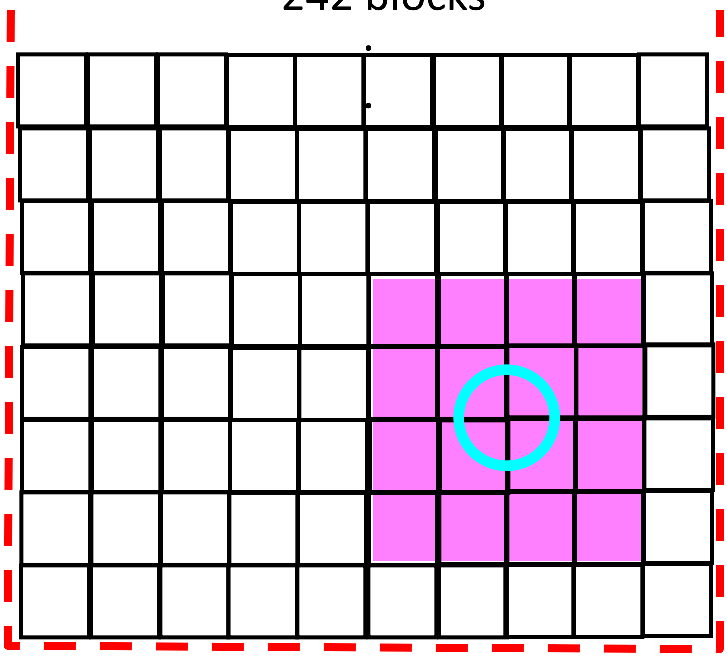
- Bigbite
- Standard Hall A equipment spectrometer used for to E02-013 GE^n,
- Same setup for 12 GeV A_1^n experiment and 12 GeV GE^n and GM^n
- Shower counter
  7x27 blocks
- Preshower
  2x27 blocks
- Analog sum on shower and preshower all modules available and used in previous experiments

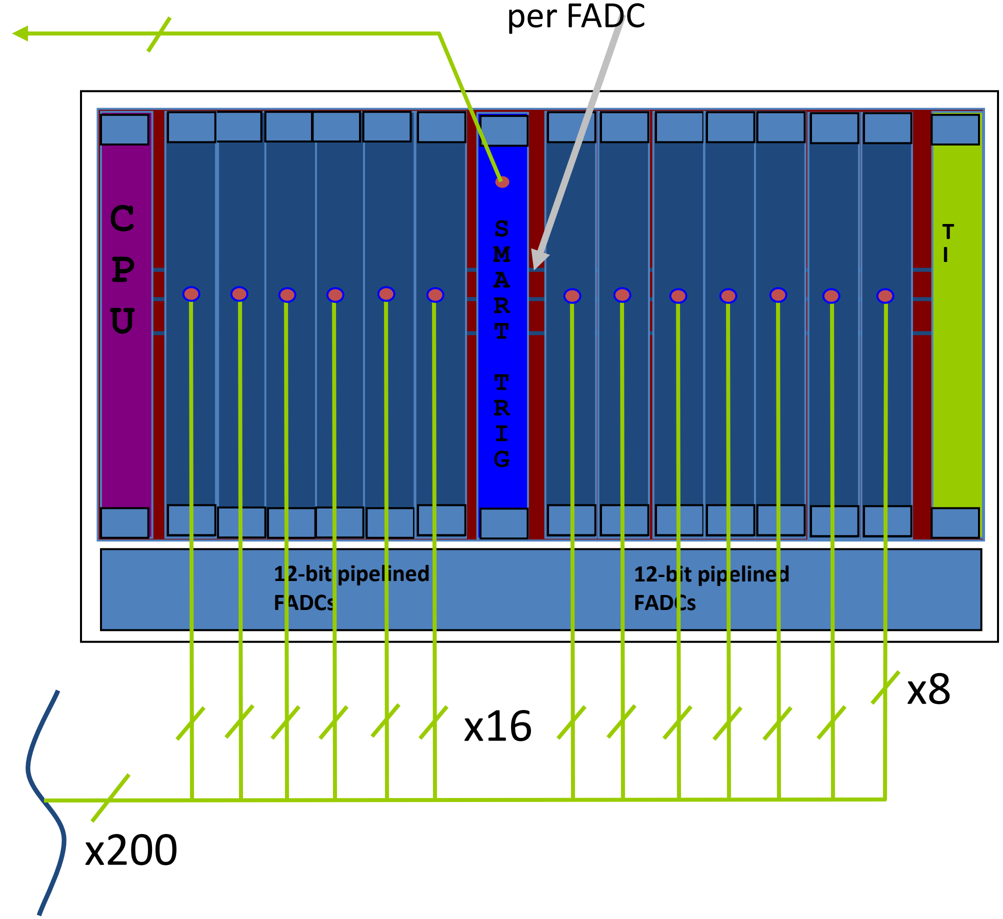


FPGA based Hadron Calorimeter HCAL Trigger

(Ole Hansen)

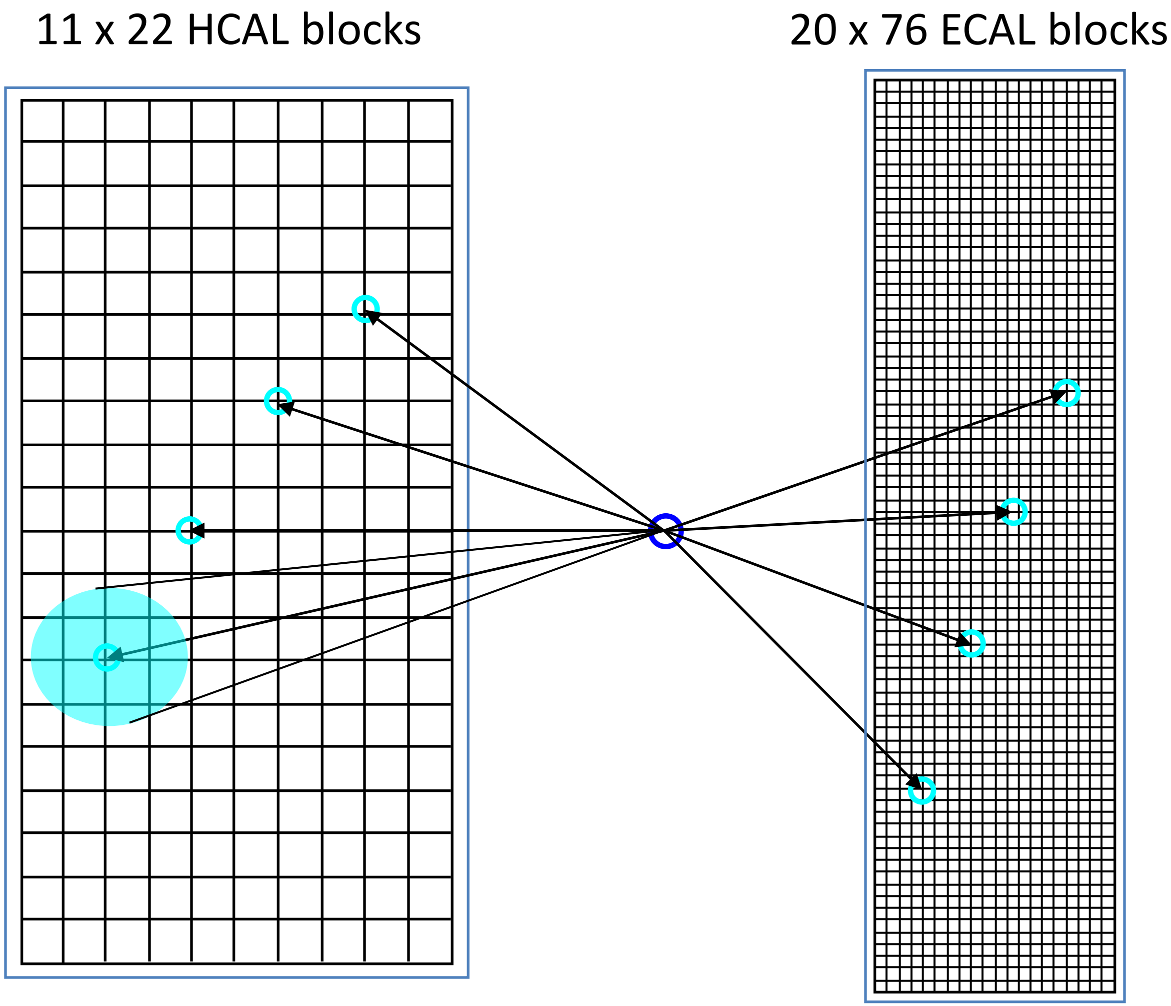
11 x22 modules
242 blocks





(CDR section F.3)

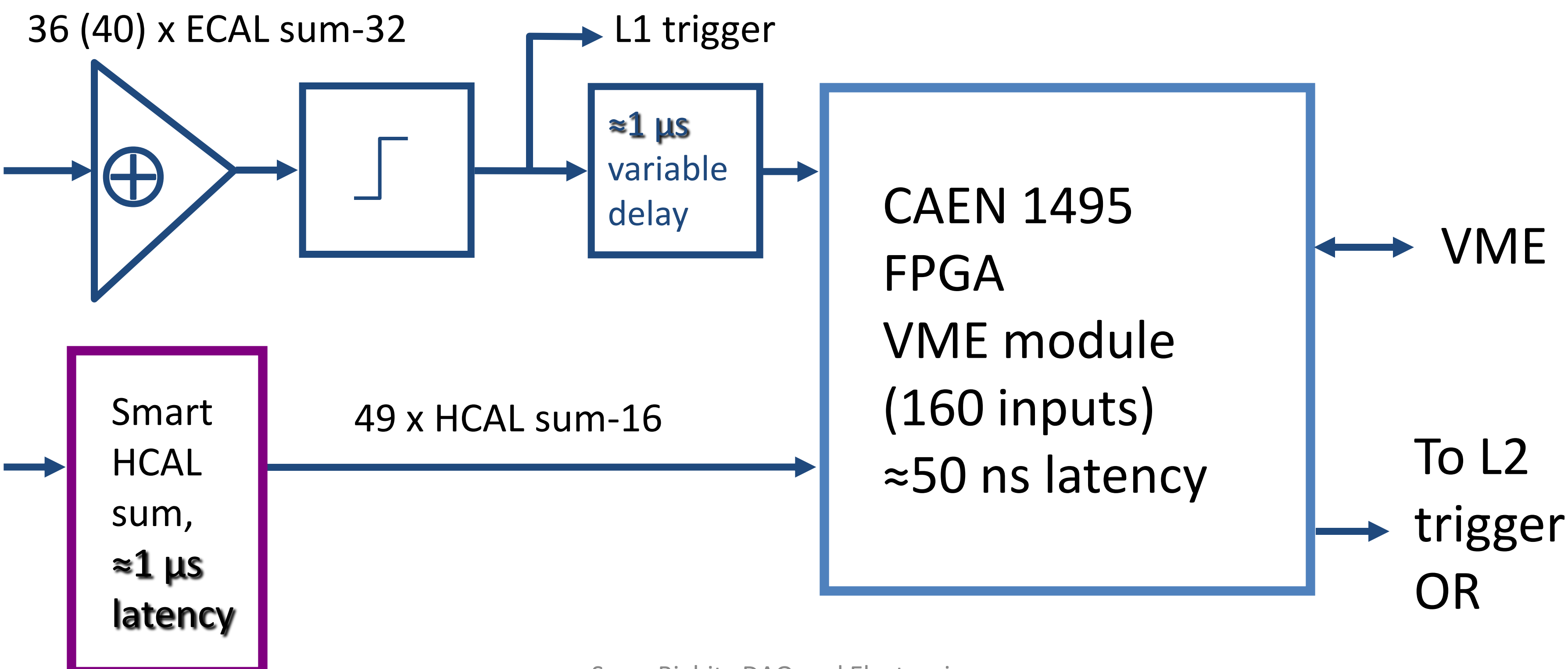
e'-p Kinematic Correlation



Using geometric correlations from elastic kinematic one can reduce final rate by a factor of 5 and tracker data by at least a factor of 3

L2 Coincidence Logic

For each calorimeter section (4x):



Tracker event size with 3 samples readout

Detector	Rate	Channels	Occupancy	Time window	Hits	Geometr ical factor	Data size	Effective data size	Data rate 3KHz Mb/s
Front Tracker	400	49000	13.5%	75ns	6615	3	52Kb	14.3Kb	43
Second Tracker	130	13600	7.4%	50ns	1010	5	8Kb	1.6Kb	5
Third Tracker	64	13600	3.6%	50ns	490	5	4Kb	0.8Kb	2
Electron arm GEM	173	12000	2.4%	50ns	288	1	2.3Kb	2.3Kb	6
Calorimeters					125		0.5Kb	0.5Kb	1.5
						Total	**67.8Kb**	**19.5Kb**	**58.5 Mb/s**

Front End and Electronics

- Available from Hall
  - HV power supply: Lecroy 1461 used in previous experiments
    Number of modules sufficient to power all the detectors
- UVA
  - All HV system for the GEMs
- Glasgow : NINO chips amplifier discriminator
- Electronics from SBS project
  - GEM : APV25 + Multipurpose Digitizer INFN VME readout, all chips procured. VME readout and front end procure build and test by NSU

MPD APV25 INFN readout

- Multi Purpose Digitizer
- GEM readout
- Up to 16 APV by board
  2048 channels / board
- Latency :

t_{APV} = 141 x number_of_sample / 40 MHz = 11 us

- Buffered
- VME320 board

Hall A DAQ Infrastructure

- CODA 3
  - Developed by JLAB for high rates experiments
  - Support event blocking and pipe lined electronics
  - Option for L3 farm for data reduction
- Network upgrade completed in 2010
  - 1 Gigabit line = 125 Mb/s
- Computer
  - Upgrade for current experiment (multicore processor)
  - SAS + Raid drives : (single drive have typical rate of 100 Mb/s scales with number of disks) 200 Mb/s setup
  - Silo storage : upgrade ethernet line – Limit tape price

Trigger & DAQ Collaboration

- Rutgers / New Hampshire
  - CAEN v1495 FPGA coincidence logic (hardware from Drell Yan experiment)
- Jefferson Lab
  - HCAL digital summing electronics
  - DAQ setup
- Norfolk State
  - 2nd and 3rd tracker front-end electronics
- INFN Rome & Genova
  - GEM readout electronics & DAQ interface
- Glasgow
  - NINO Front End electronic for PMTs

Part of WBS
SBS projects

Research Man Power

- GEM readout APV25 / VME
  - INFN : Evaristo Cisbani, 1 technician
  - NSU : Mahbub Kandaker, Vina Punjabi
- Front End NINO chips
  - Glasgow : John Annand
- Hadron calorimeter trigger and trigger logic
  - Ron Gilman, 1 postdoc, 1 student
  - Jefferson Laboratory : Ole Hansen, Alexandre Camsonne
- Electron calorimeter trigger
  - Jefferson Laboratory : Mark Jones, Alexandre Camsonne
  - William and Mary : Charles Perdrisat
- Hall A infrastructure
  - DAQ computer : Ole Hansen
  - Network : JLAB network

Time line

- 2011
  - Hall A computer upgrade
  - FADC tests
  - Intel VME CPU test : reach 10 KHz rate with Fastbus for g_2^p
- 2012
  - GEM + APV25 GEM tests during g2p
  - FADC tests (achieve 100 KHz trigger rate for Compton for PEPPO)
  - Receive BELLE Fastbus electronics + MQT
  - 4 JLAB FADC250
- 2013
  - Small scale setup for testing : FADC + trigger + Fastbus + APV25
  - All APV25 and MPD for GE^n built and tested by NSU
- 2014
  - MPD GEM electronics installed on detectors for GE^n
  - Start Gep electronics
  - Start Hadron Calorimeter Trigger implementation
  - A_1^n :
    - Full scale test of GEM
    - Digital Trigger electronics test parasitic
- 2015
  - GEM DAQ integration
  - Full scale system deployed ready for GE^n
- 2016
  - Hadron Calorimeter complete
  - Full DAQ setup
- 2017
  - Ready for GE^n

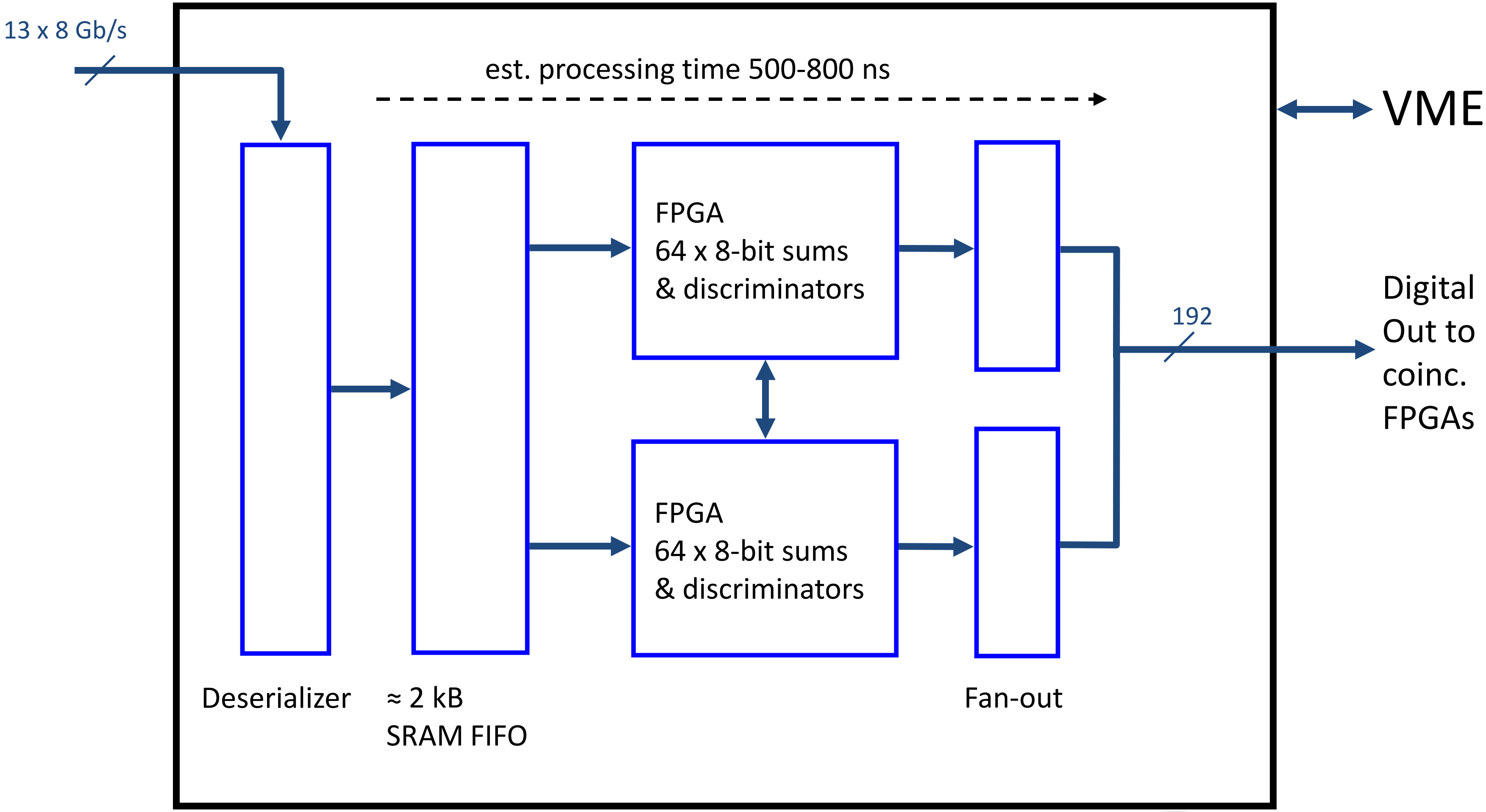
More details in J. Lerose
Management talk for detailed cost and schedule

Conclusion

- Use of existing electronics for electron arm triggers and readout
- Electronics built as part of the project
  - GEM readout
  - Hadron calorimeter trigger capitalizing on Hall D developments
  - Electronics will be useful for future Hall A experiments
- Trigger logic and readout finalized
- High occupancy but geometrical correlation from elastics kinematics helps for the Form Factor Experiments
- Validation of the setup performances and data rates with different test setups and simulations will be done
- No particular issues foreseen

Backup slides

“SMART Trigger” Module



New Hall D type JLAB Electronics

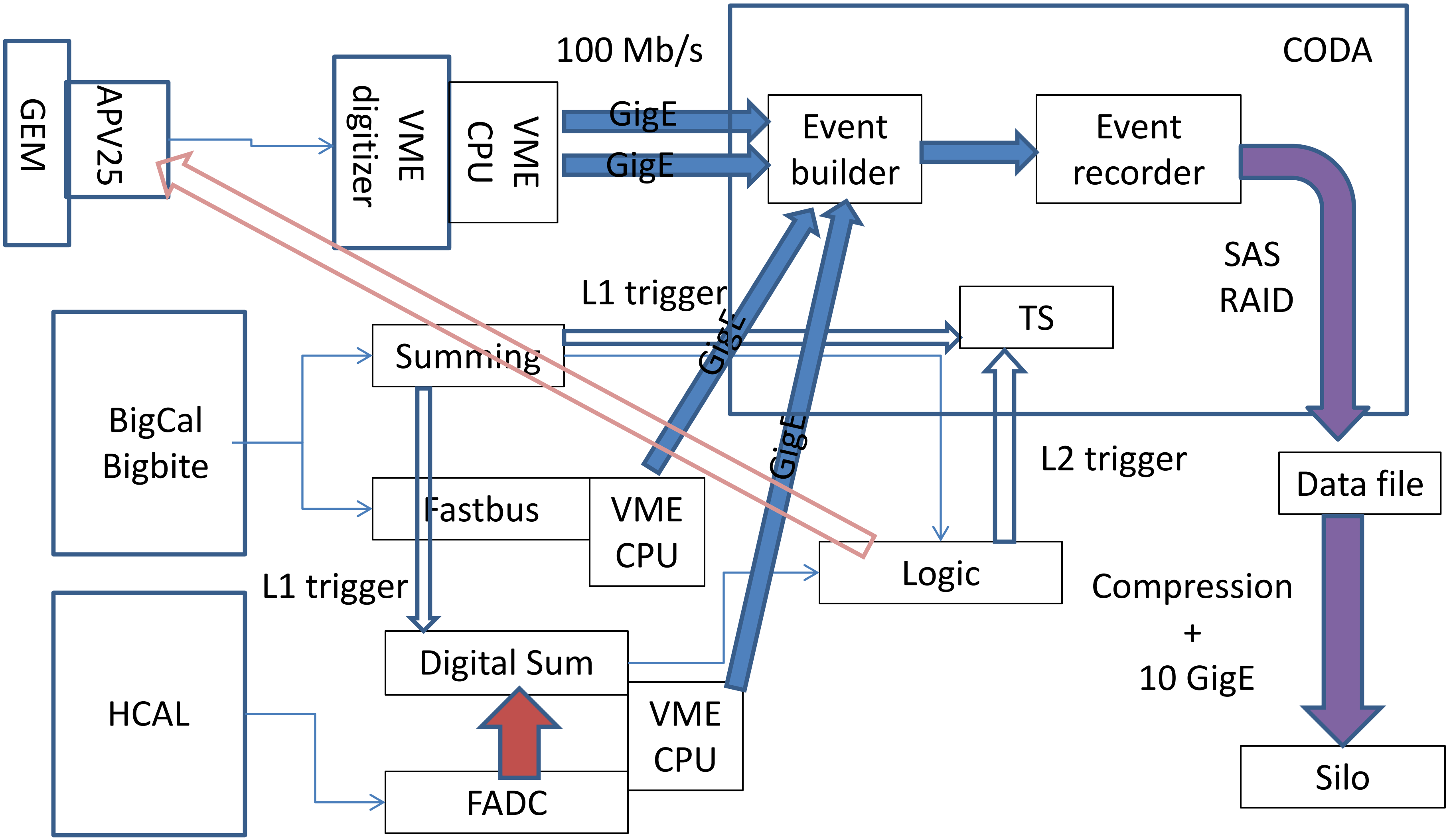
- Under development by JLab DAQ group
- Fully pipelined
- 200 kHz L1 trigger rate capability
- Synchronous trigger distribution, 250 MHz ref. clock
- VME64x front-end crates with support for
  - High-speed readout modes (2eVME, 2eSST) up to 200 MB/s
  - On-module event buffering - up to 200 events
  - Gigabit uplinks to event builder
- CODA 3 software
- Will use some of this technology + custom modules

JLAB FADC 250

- Deployed in Hall A Moller
- Developed for injector Mott and Compton transmission : 100 KHz of triggers

- Future test stand with Hall D summing module as starting point for Calorimeter trigger

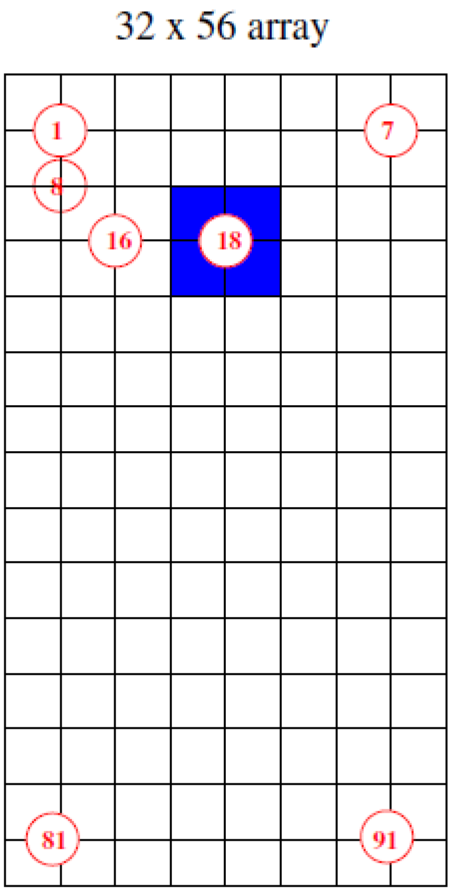
Data flow


GEM
APV25
VME
digitizer
VME
CPU
100 Mb/s
GigE
GigE
CODA
Event
builder
Event
recorder
SAS
RAID
L1 trigger
GigE
TS
Summing
BigCal
Bigbite
Fastbus
VME
CPU
GigE
L2 trigger
Data file
Logic
L1 trigger
Compression
+
10 GigE
Digital Sum
VME
CPU
HCAL
FADC
Silo

BigCal trigger

- 112 sum over 4 x 4 blocks
- 28 sums over 8 x 8 blocks

- Or of threshold on sum of 64 blocks
- Signal sent to ADC and TDC



Belle Q to T

- MQT300
- Gives one timing signal and another time for the edge corresponding to amplitude
- Easier to delay signal
- Use only 1877S
- Reduce max encoding from 9 us to 6.5 us
- Use of several gain sent on different channels for increased resolution and reduced latency

Fastbus

- Big Cal
  - 1550 channels = 12 1877s TDC modules for time
  - 1550 channels = 12 1877s TDC modules for amplitude using MQT
  - Use several crates for parallel read out to overcome Fastbus 40 Mb/s backplane limit
  - Dead time only coming from Front End Busy using buffering
  - Fast clear from L2 with latency less than 1 us

Maximum data rate

- Assumption 100 channels hit per event of calorimeter
- Time
  - 1550 channels on 13 TDC : ~ 7 channels = 1.75 us
  - 112 sums over 16 : one TDC : ~ 6 channels = 1.75 us
  - 28 sums over 64 blocks : one TDC : ~ 4 channels = 1.75 us
- Amplitude
  - 1550 channels on 13 TDC : ~ 7 channels = 2 +1.75 = 3.75 us
  - 112 sums over 16 : one TDC : ~ 6 channels
  - 28 sums over 64 blocks : one TDC ~ 4 channels

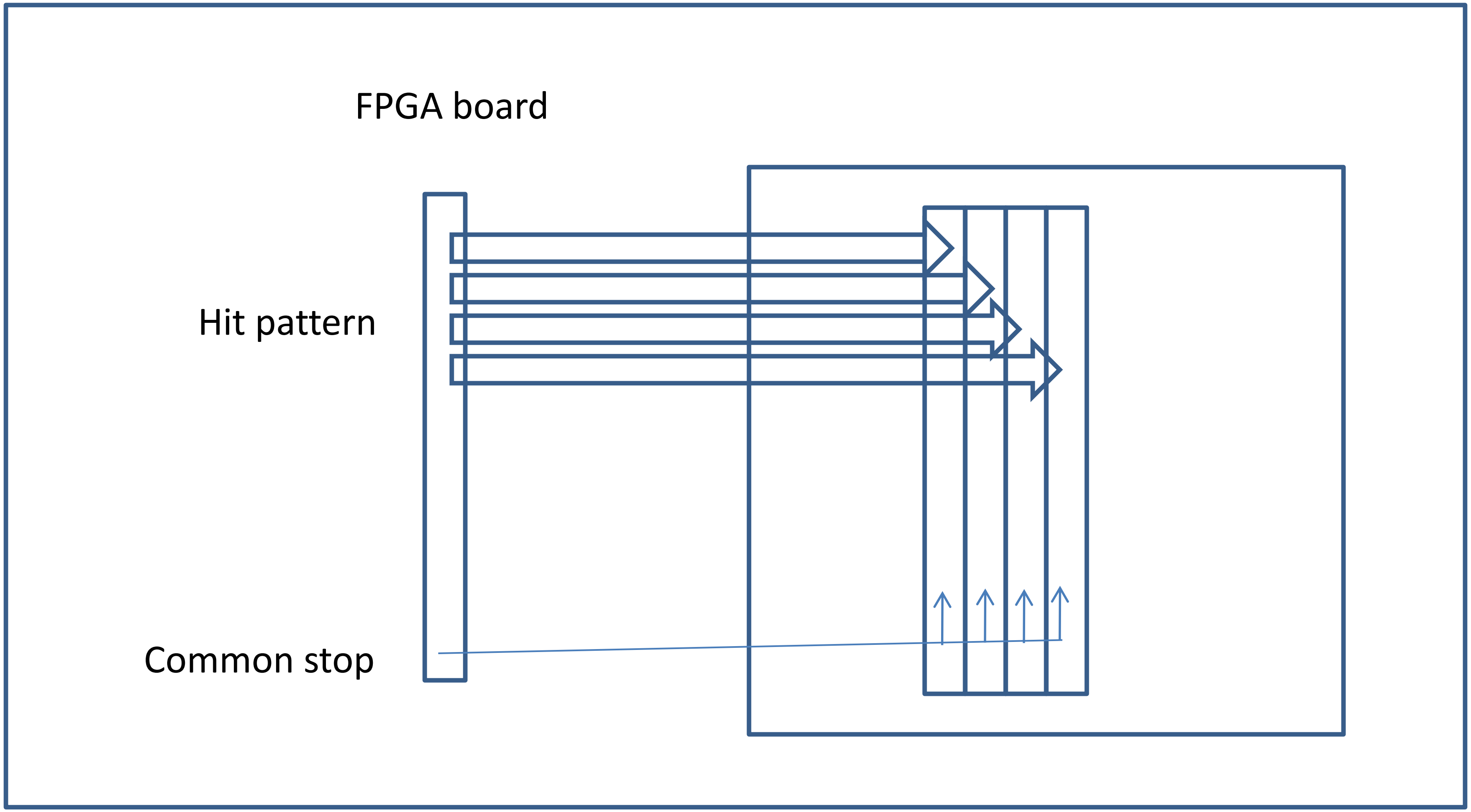
Max encoding time 3.75 us

Maximum data rate

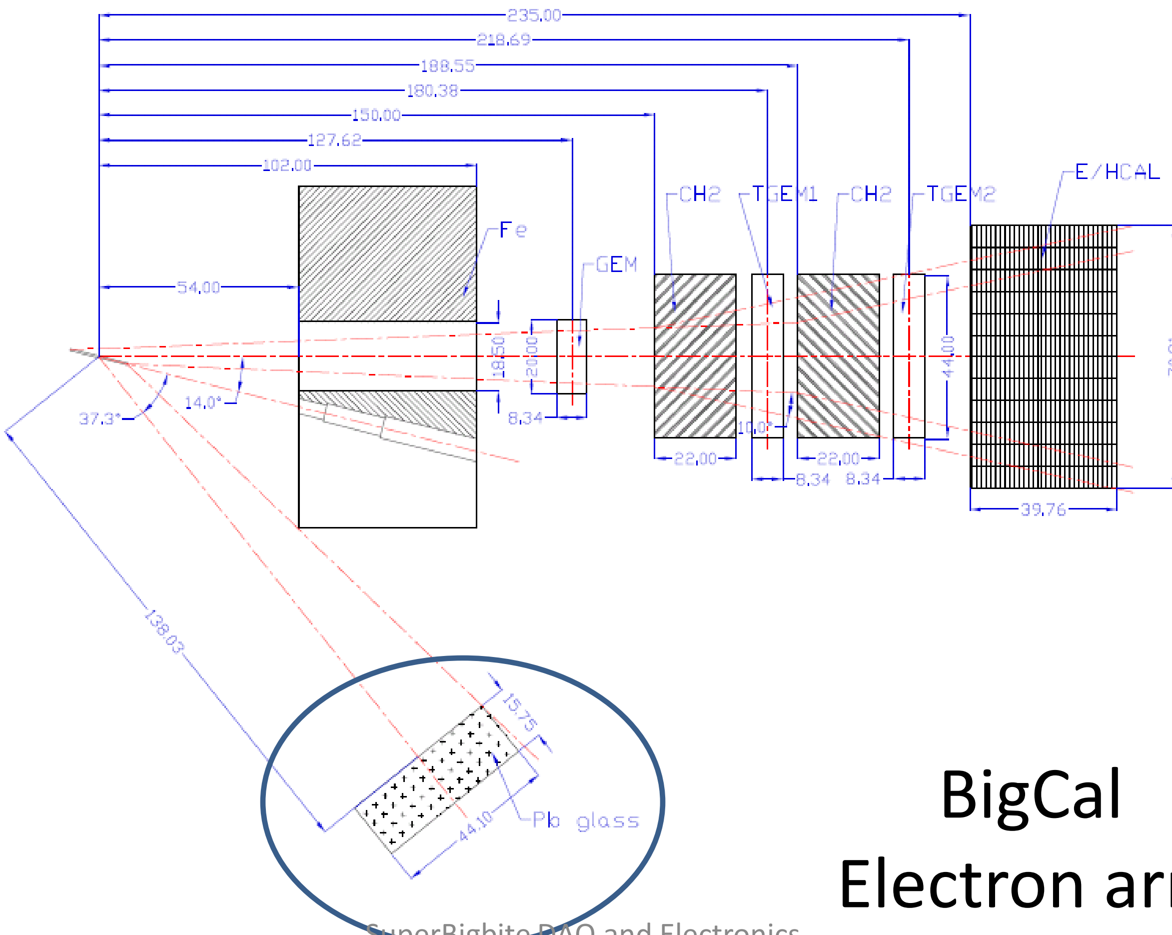
- Maximum rate to be tested
  - Typical 4 KHz
- Try new Intel VME CPU
  - Multicore GE VXB601

- If bottle neck on Fastbus (currently factor 10 margin assuming 100 calorimeter blocks read)
  - Increase number of crates
  - Use event blocking for optimized readout

Test setup

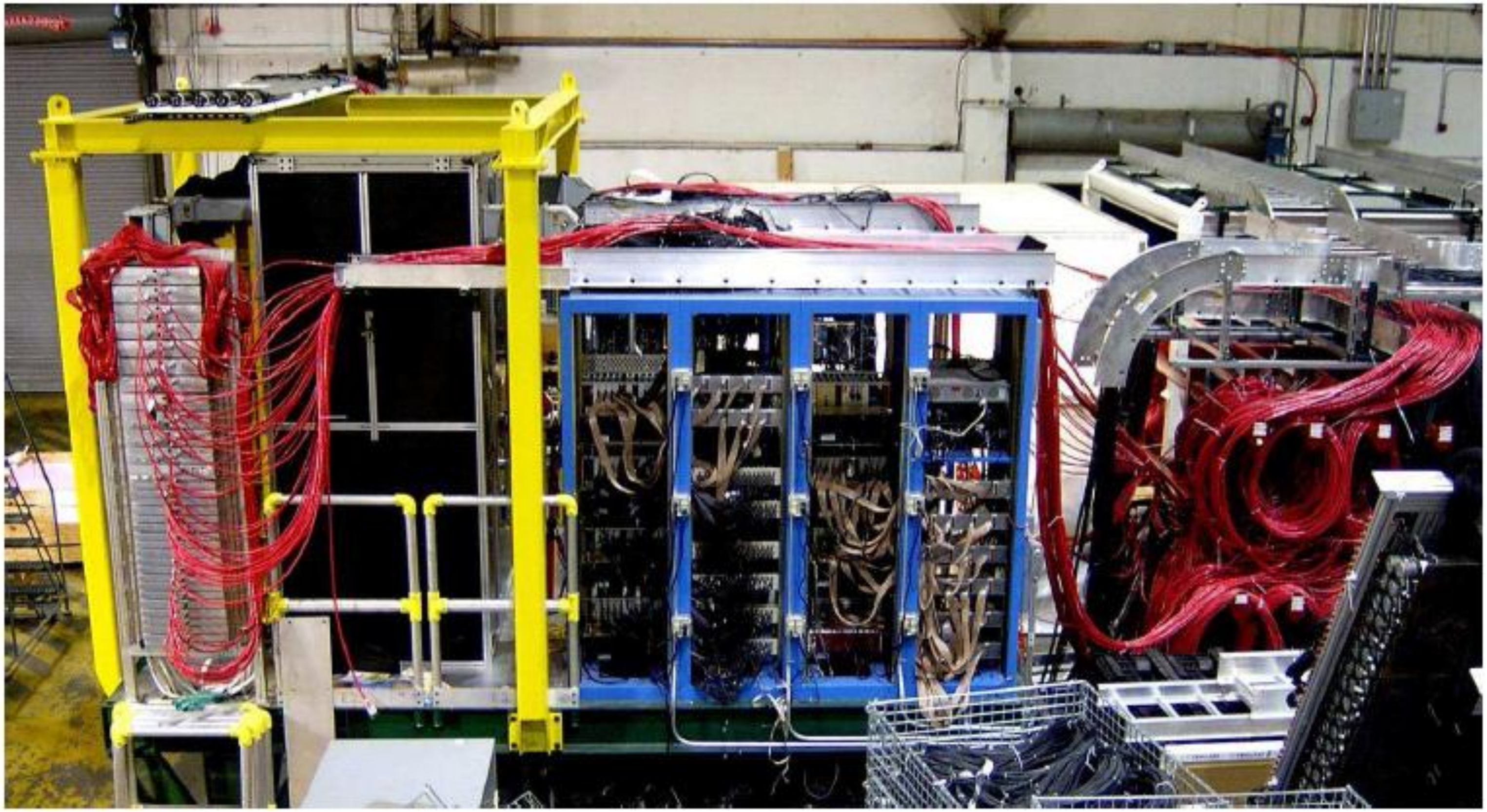


Big Cal



BigCal
Electron arm

Big Cal



1877S

- 10 Megawords /s = 40 MB/s
- 16 Hits/channel
- Conversion time : 1.2 us + 50 ns/hit
  1.75 us Min 7.6 us Max
- Suppression : windows with steps of 8 ns
- **AS-AK Handshake Time:** 125 nsec typical, 150 nsec maximum.
  DS-DK Handshake Time: 65 nsec typical, 75 nsec maximum (Block Transfer).

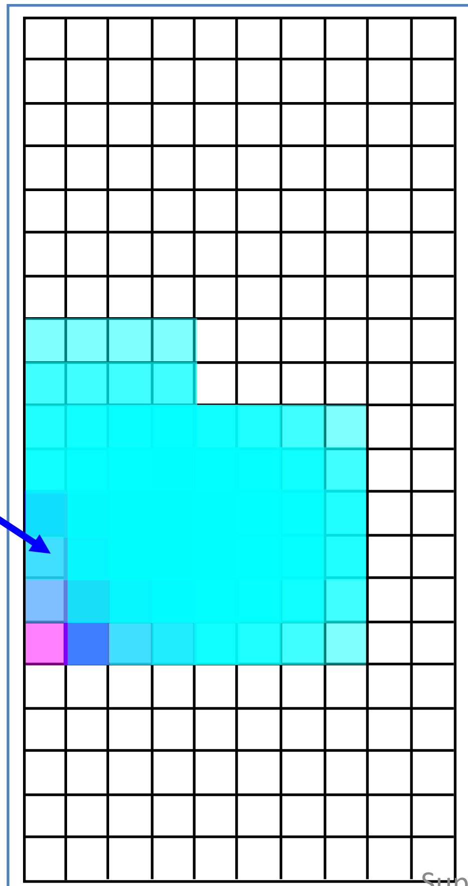
(CDR section F.3)

Calorimeter Sums

10 x 20 HCAL blocks

7x17 = 119
sum-16

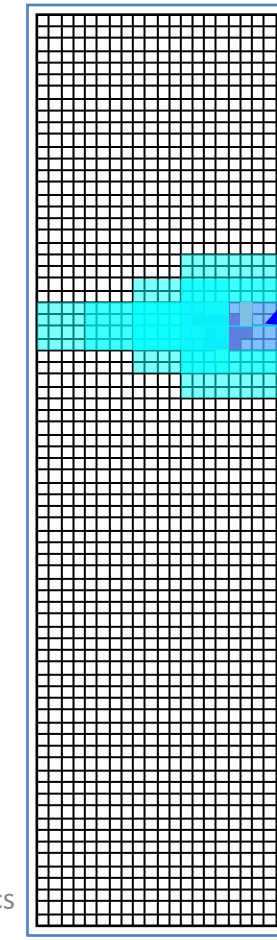
sum-16



20 x 76 ECAL blocks

4x37 = 148
sum-32

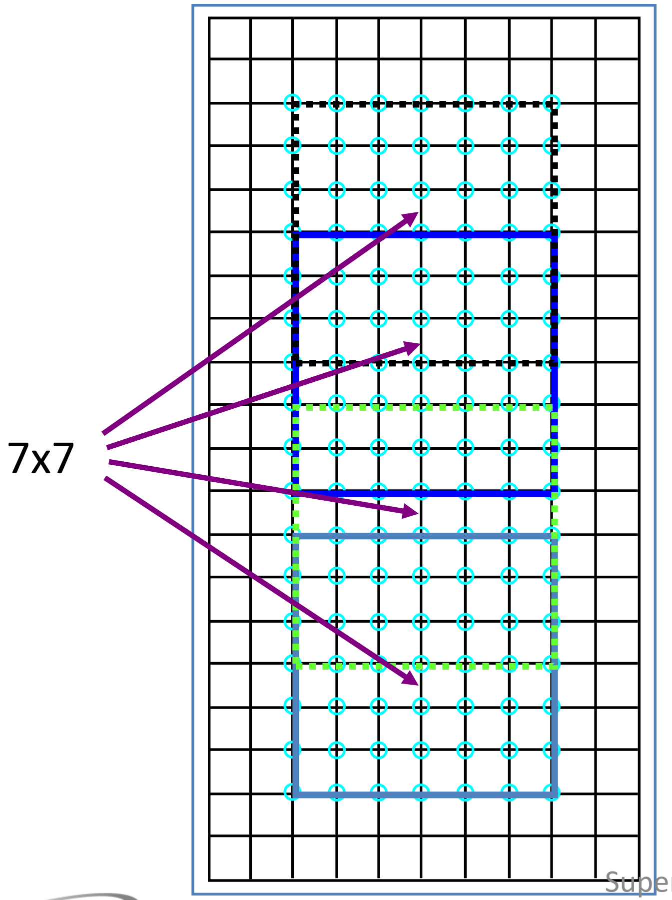
sum-32



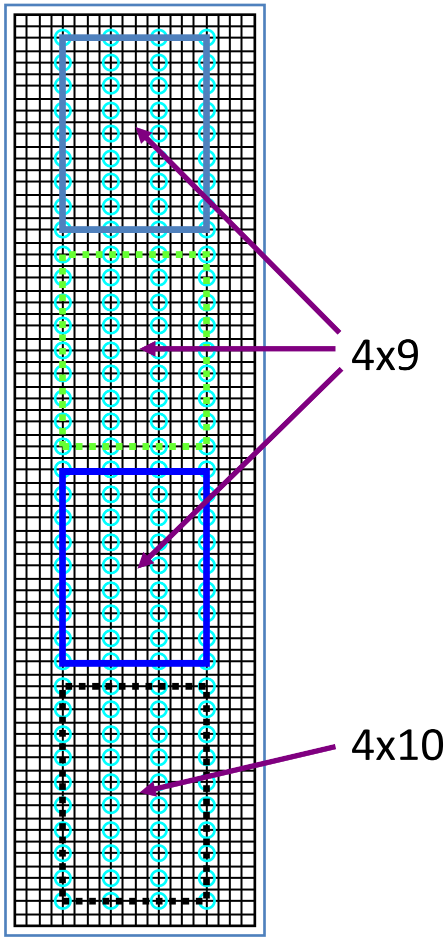
(CDR section F.3)

Calorimeter Sectioning

HCAL sums of 16: 7x17 = 119

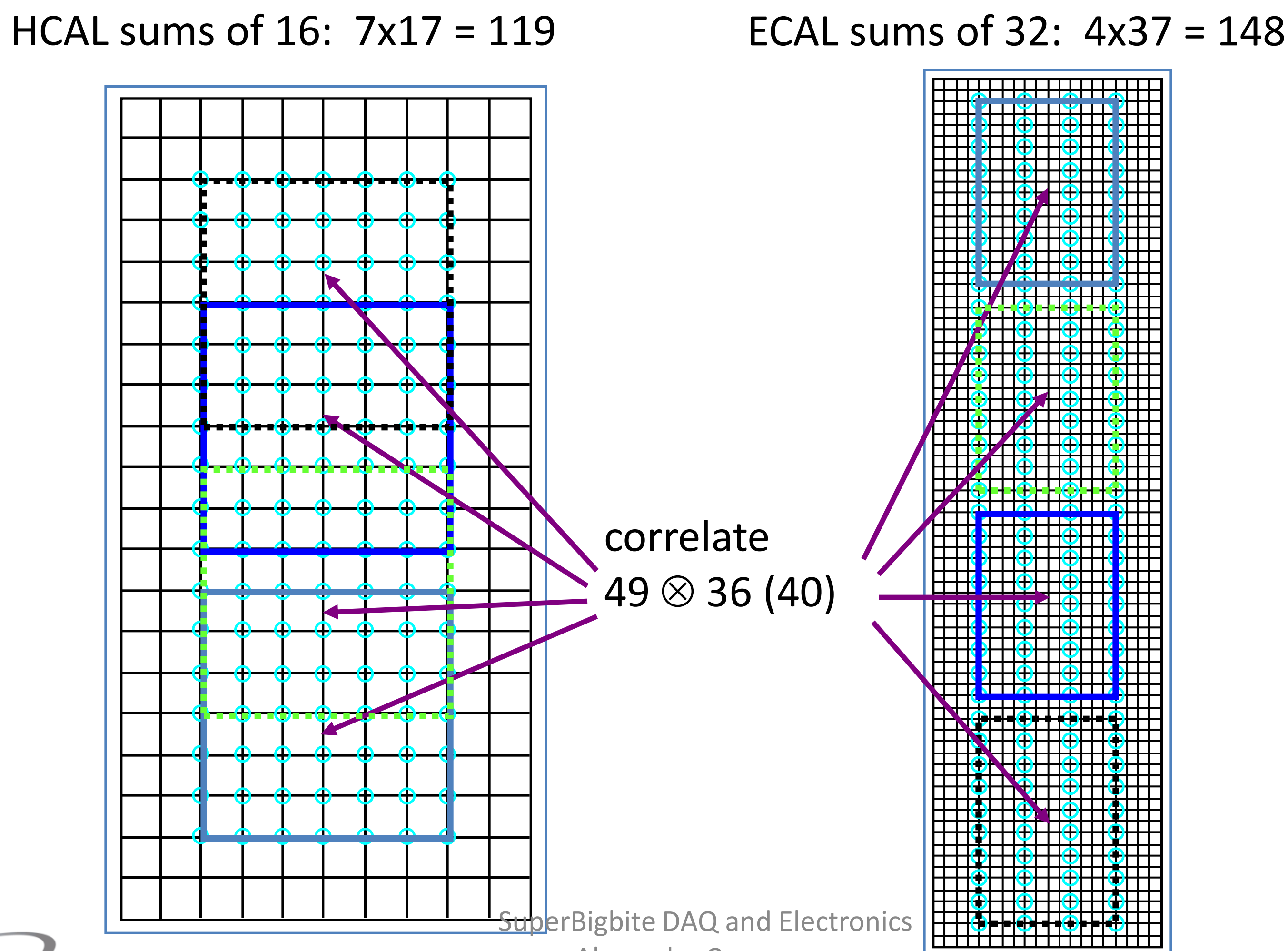


ECAL sums of 32: 4x37 = 148



(CDR section F.3)

Calorimeter Sectioning



Rate reduction: x5

1881M

- 10 Megawords /s : 40 Mb/s
- 16 Hits/channel
- Conversion time : 12 us 13 bit – 9 us 12 bit
- **AS-AK Handshake Time:** 125 nsec typical, 150 nsec maximum.
  DS-DK Handshake Time: 65 nsec typical, 75 nsec maximum (Block Transfer).

Evaluated bottlenecks

- Frontend conversion : 1.75 us to 7.6 us
- Fastbus : 10 Megawords/s
- CPU bus : 40 to 80 Mbytes/s
- Network : Gigabit Ethernet 125 Mbytes/s (typical 80 Mb/s for each port, 2 ports used with new CPU so 160 Mb/s)

NINO Chips

- The NINO chips is an integrated amplifier discriminator board
- Read out if time and amplitude with TDC
- Analog output
- 16 channels per chip
- Glasgow in charge of Front End board development

Event size GEMs

Tracker	Area of interest for tracking, cm^2	Rate, kHz/cm^2	Strip pitch, mm	Strip occupancy, %	Number of pseudo-tracks per event	Number of strip planes
First	0.20 x 18	400	0.4	13.5	1.65×10^{-2}	12
Second	$2\pi\ 0.35^2$	130	1.6	7.4	8.7×10^{-6}	8
Third	$\pi\ 4.8^2$	64	1.6	3.6	5.2×10^{-4}	8
BigCal	$\pi\ 1.2^2$	173	1	2.4	2.8×10^{-2}	2

Amplitude 12 bit per sample

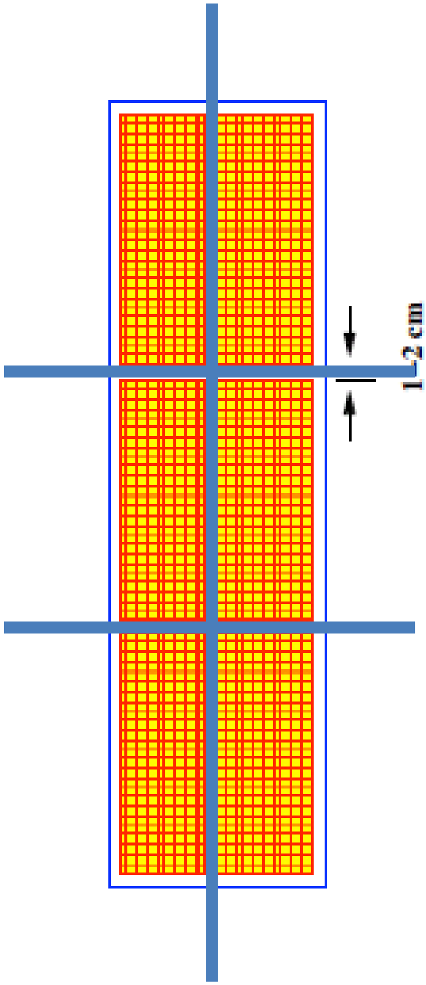
+

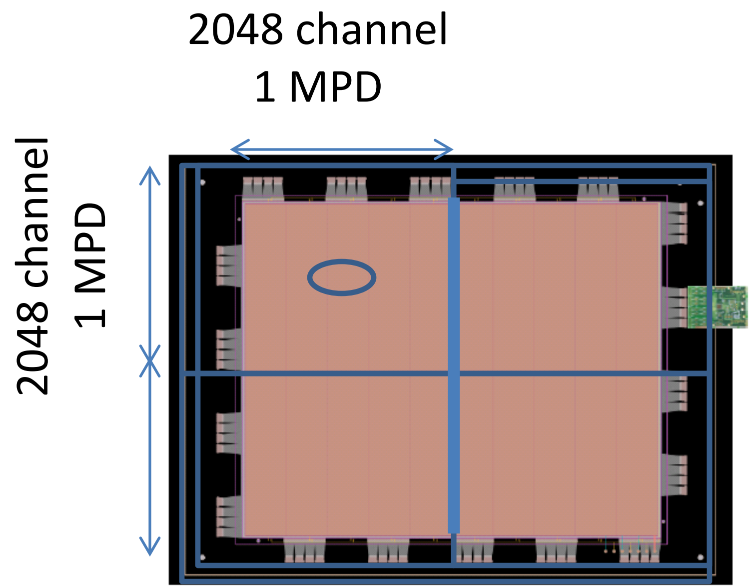
11 bit of addressing

=

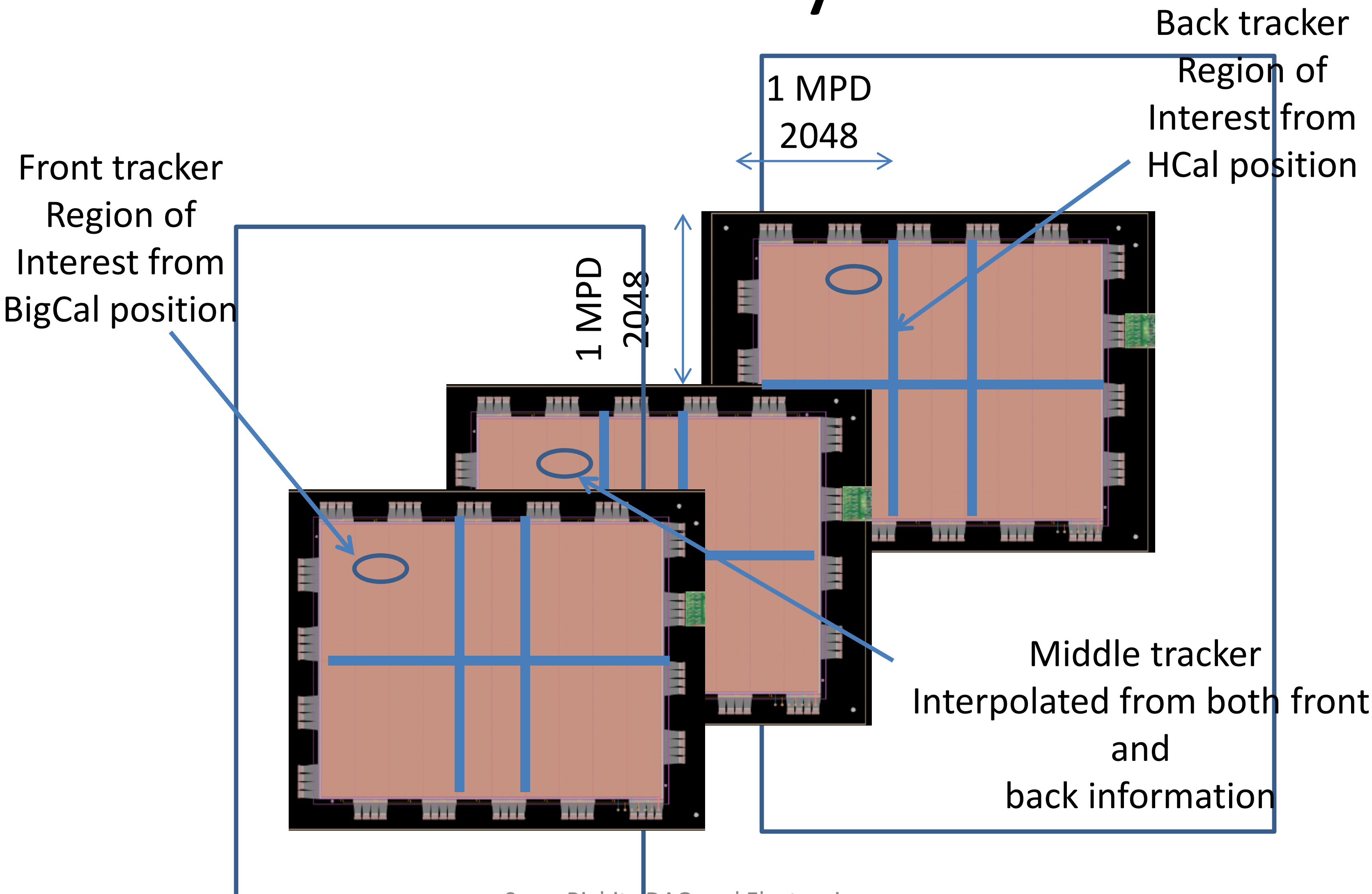
47 bytes rounded to 8 bytes (64 bit word)

Front Tracker layout

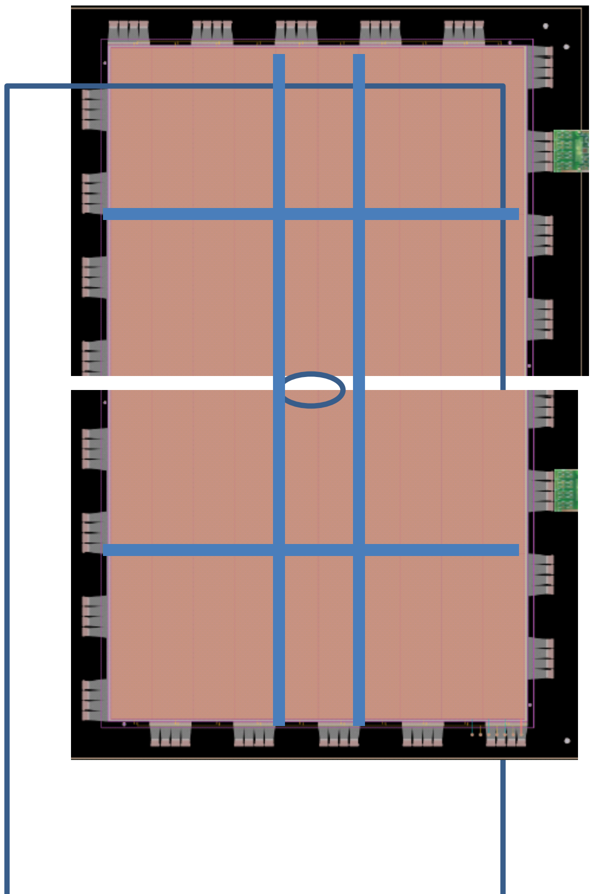




Trackers layout



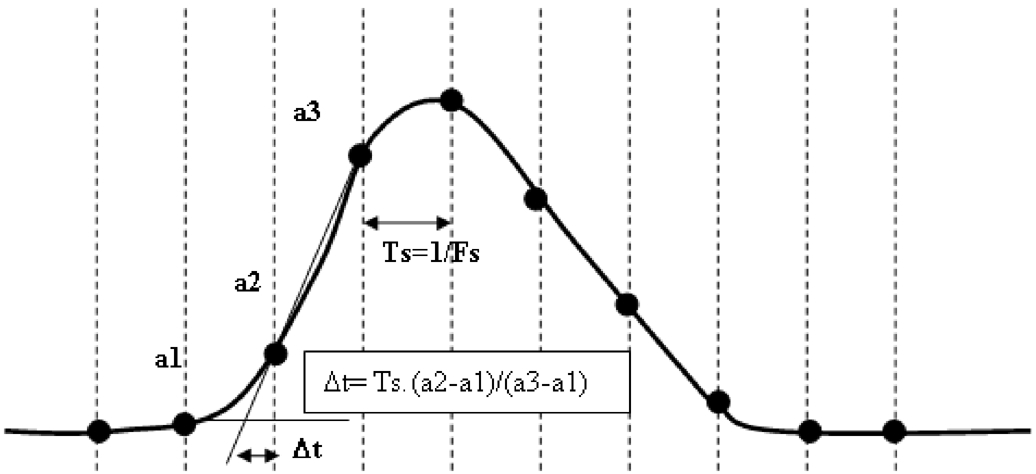
Trackers layout



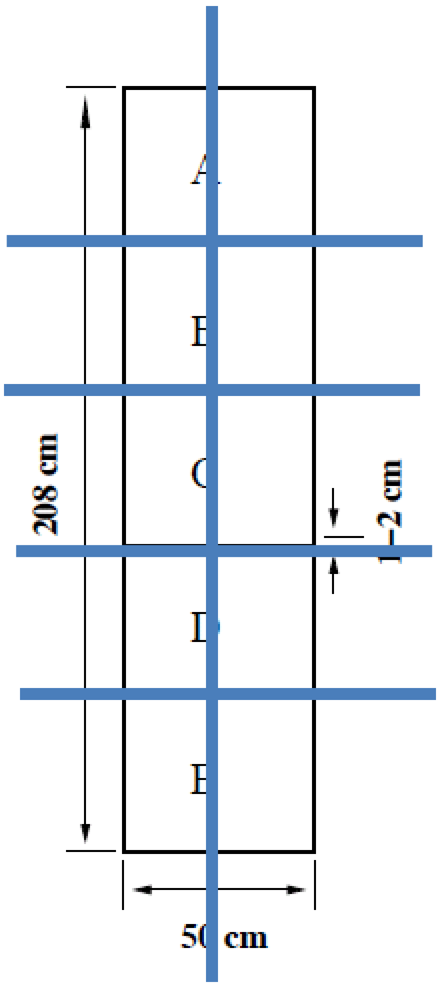
Worst case configuration

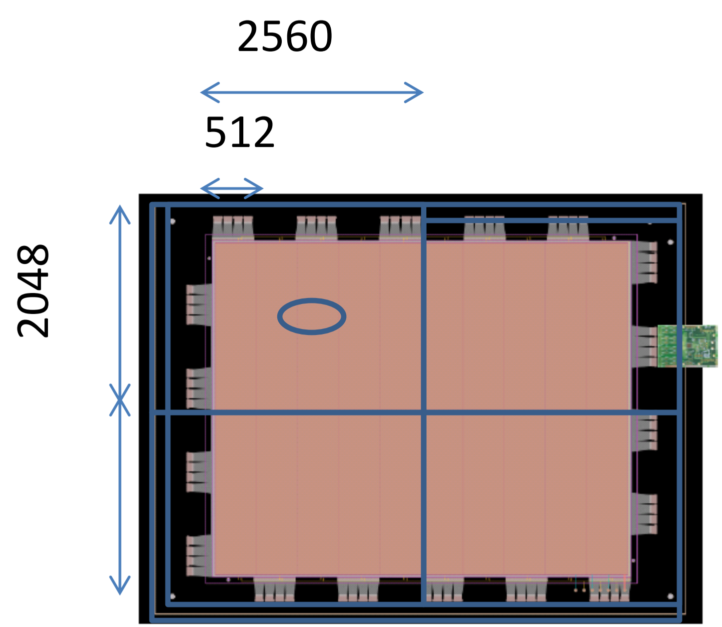
Suppression schemes

- Several algorithm can be implemented in FPGA for further data reduction
  - Thresholds
  - Timing
  - Fitting $\chi 2$
  - slope



FPP Tracker layout



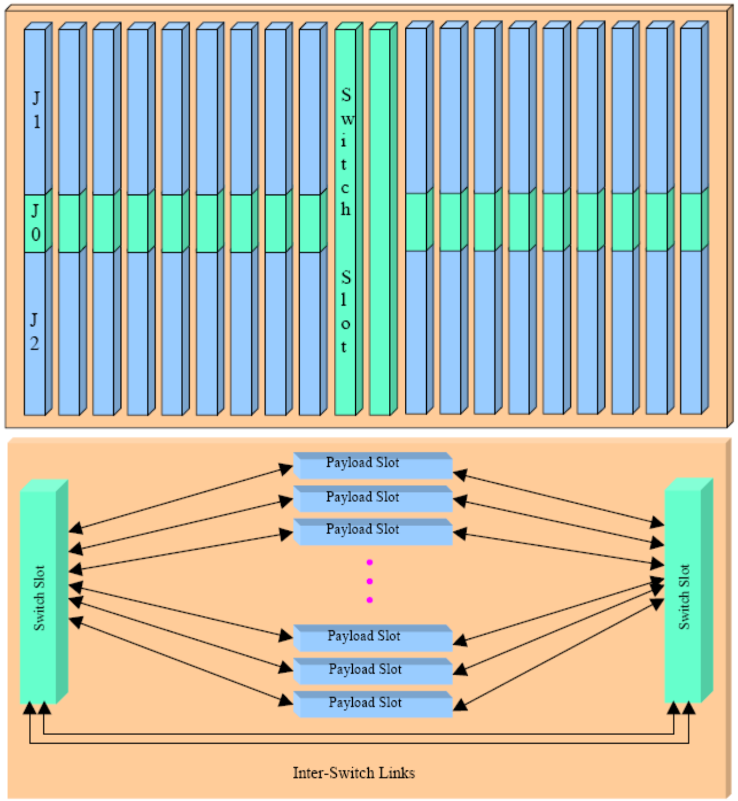


Level 1 Design

- Up to 5 detector subsystems can be used
  - FCAL/BCAL – Energy
  - Start Counter – Hits
  - Forward TOF – Hits
  - Tagger – Hits (not at high luminosity)
- Continuous computation (@ 250 MHz)
- 4 level hierarchy

  Board -> Crate -> Subsystem -> Global
- VME for the Data Path (2eSST : >200 MB/s)
- VXS for the Trigger Path
  - 18 payload slots
  - 2 switch slots (redundant star)
  - 8 serial lanes (4 each in/out) per VME slot

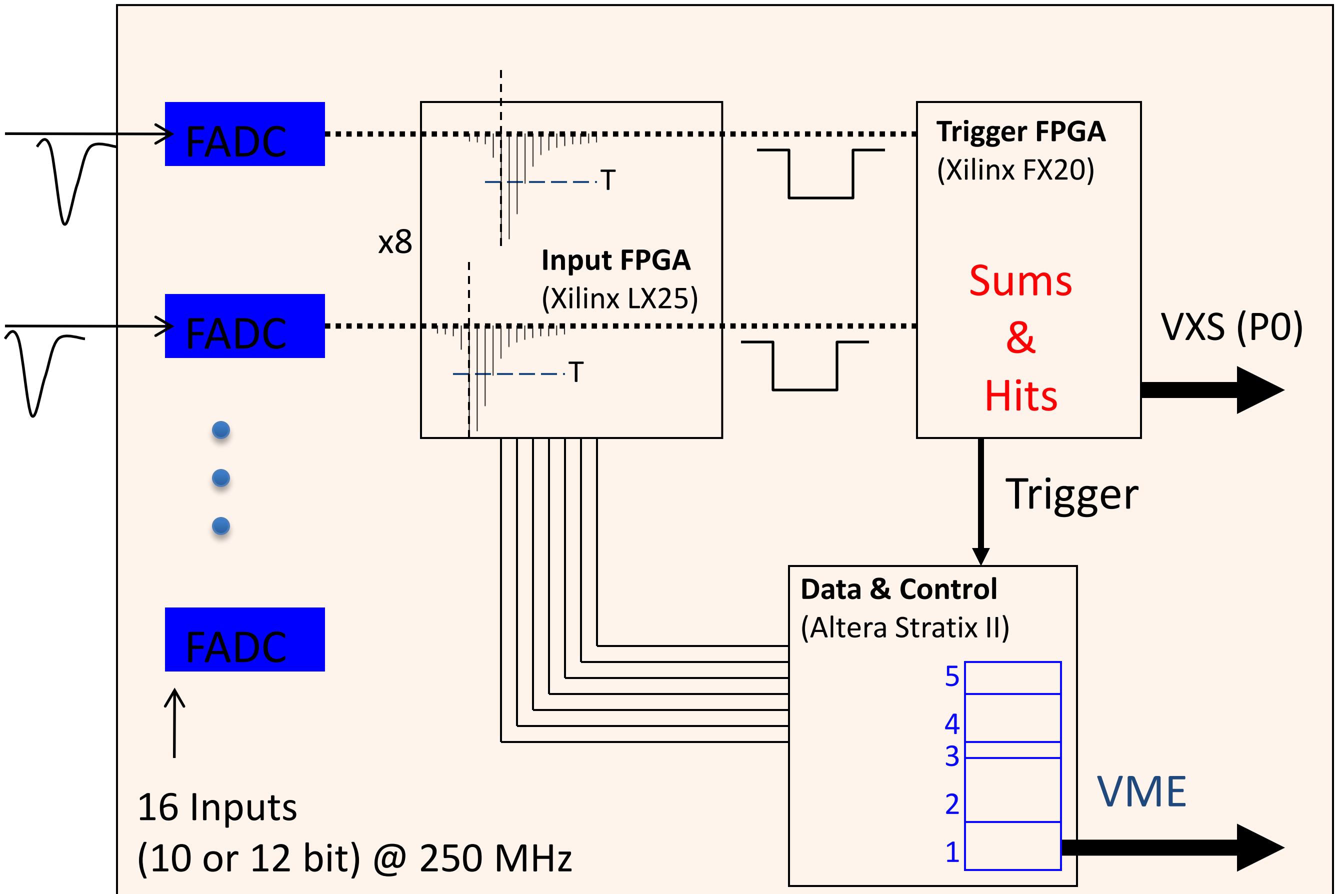
- Board level trigger starts with custom JLAB design flash ADC (250 MHz)…



VXS (VITA 41 standard)
VME64x + high speed
serial fabric on J0

JLAB 250 MHz Flash ADC

- Pipeline trigger/data (8 microsec lookback)
- User downloadable (via VME) code for Input/Trigger FPGAs



Rocket I/O
Aurora protocol
x2 lanes bonded
2.5 Gbps/lane
8/10 bit encoding
Data: 500 MB/s

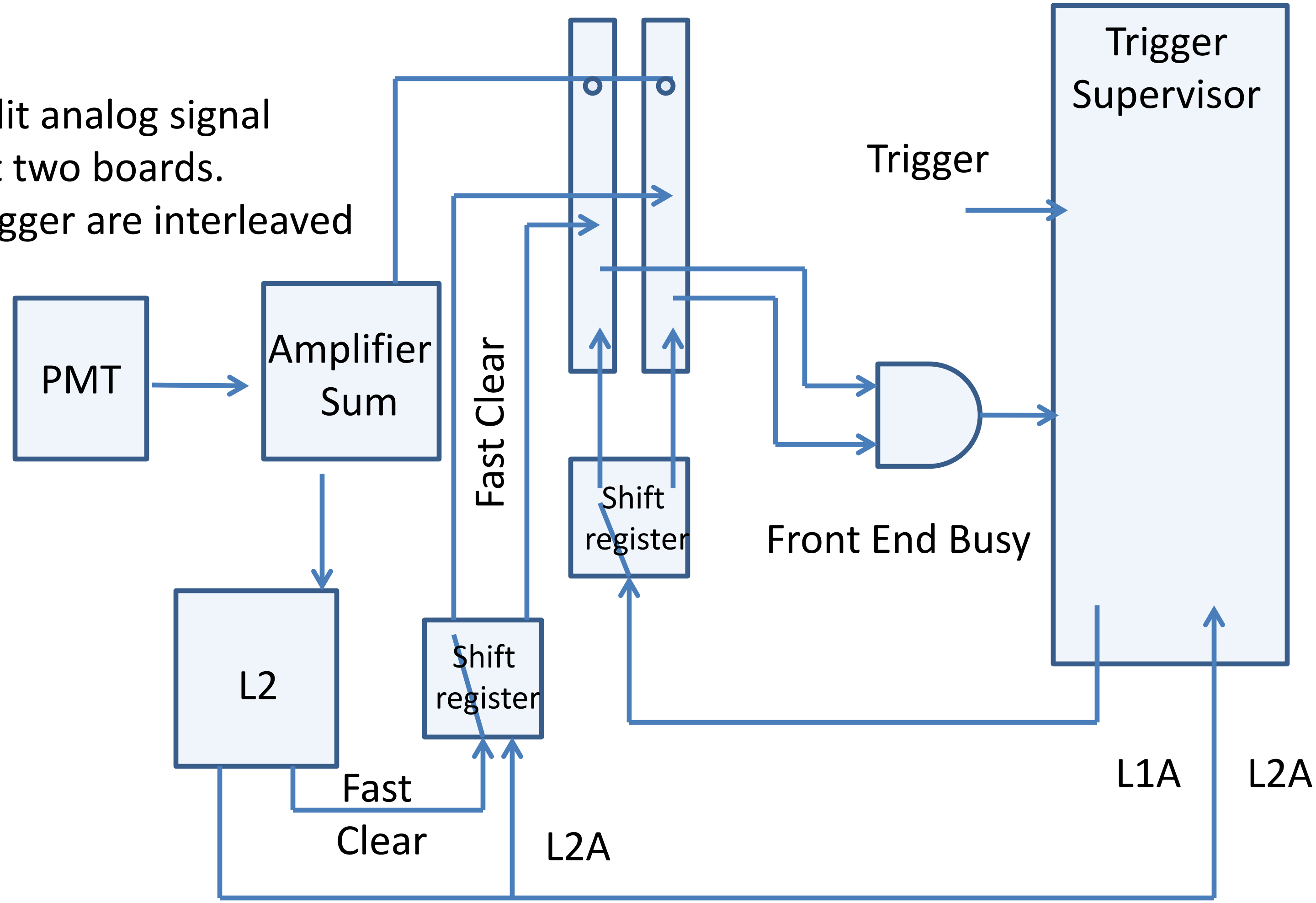
2eSST
Data: 200 MB/s

Hall A 12 GeV DAQ

Milestone	Planned
Implement 1190 and 1290 TDCs on HRS	Oct-11
Implement Fastbus upgrade with Intel Quad cpus	Nov-11
Complete the Design of Test Stand for Pipelined Electronics	Dec-11
Obtain prototype TIR boards, new ROC and EB components for CODA 3	Jan-12
Complete the Design of the Delay Modules (Ben Raydo)	Feb-12
Parts for Test Stand Delivered (FADC, TDCs, TIR, etc)	Mar-12
Test of Delay Module Prototype Completed	Apr-12
Initial Testing of Pipelined Electronics, informing final design	May-12
Preliminary Design of DAQ and Trigger	Jun-12
Order Delay Modules and other Trigger Modules	Jul-12
Completed Tests of Pipeline Electronics	Aug-12
Final Design of DAQ and Trigger	Sep-12
Order ADCs and TDCs (at this point, looks like Jlab FADC and CAEN 1190)	Oct-12
Order Crate Trigger Supervisor, Subsystem Decision Modules, etc.	Nov-12
Order Fibers and Gigabit Ethernet	Dec-12
All DAQ and Trigger modules delivered	Jan-13
Analysis Software Upgrades Completed (based on Test Stand)	Feb-12
Assembly of Full DAQ System Complete	Mar-12
Preliminary Tests of Full DAQ System	Apr-12
Final Tests of Full DAQ System	May-12

Module flipping

Signal is split analog signal
and sent two boards.
Readout and trigger are interleaved



Module flipping

- Signal split after amplifier between several modules
- Large quantity of Fastbus will be received from BELLE
- L2 in 800 ns max, Fast Clear 1 μs = 1.8 μs latency
- Flipping scheme reduces Front End deadtime with 200 kHz L1 rate from 36 % to 13%