Making Fastbus Faster

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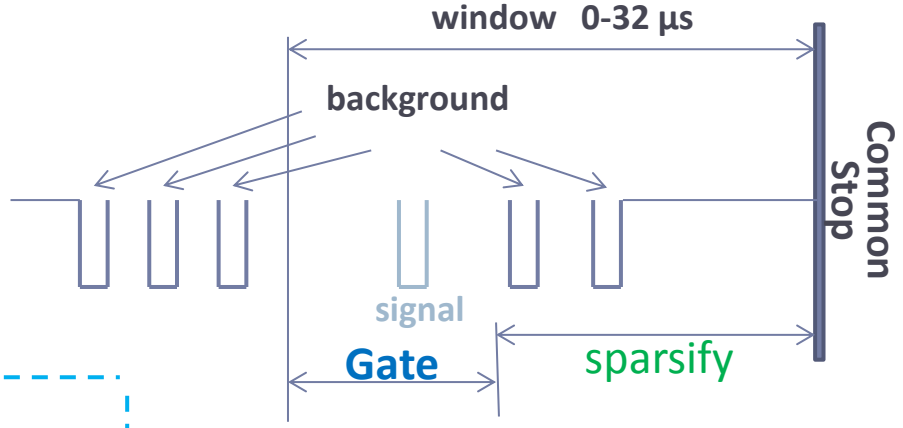
I. Sparsification

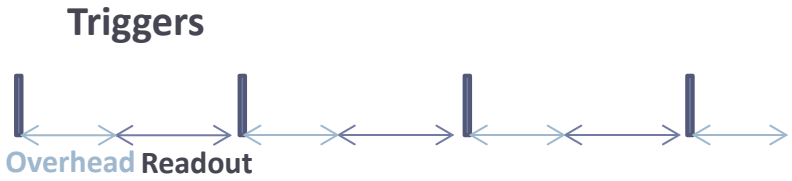
Throws out background hits



Status: tried, works

II. Event Blocking

Blocklevel=4 should work with pipelining VME

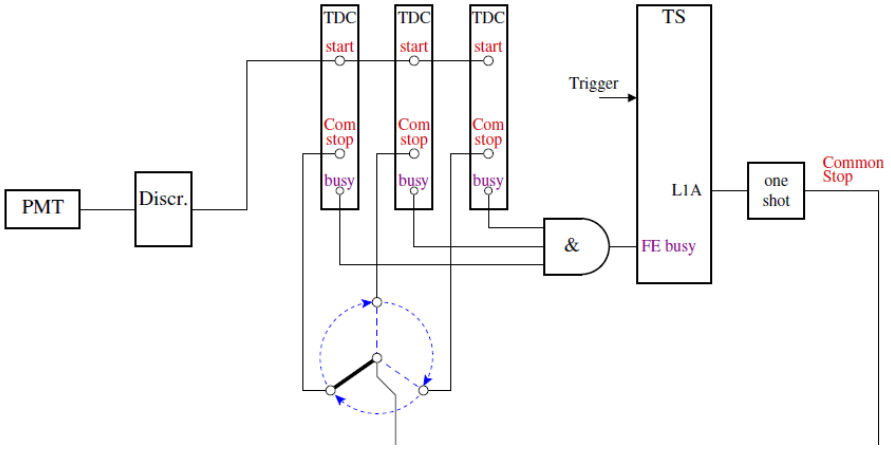


Buffers the deadtime and reduces overhead

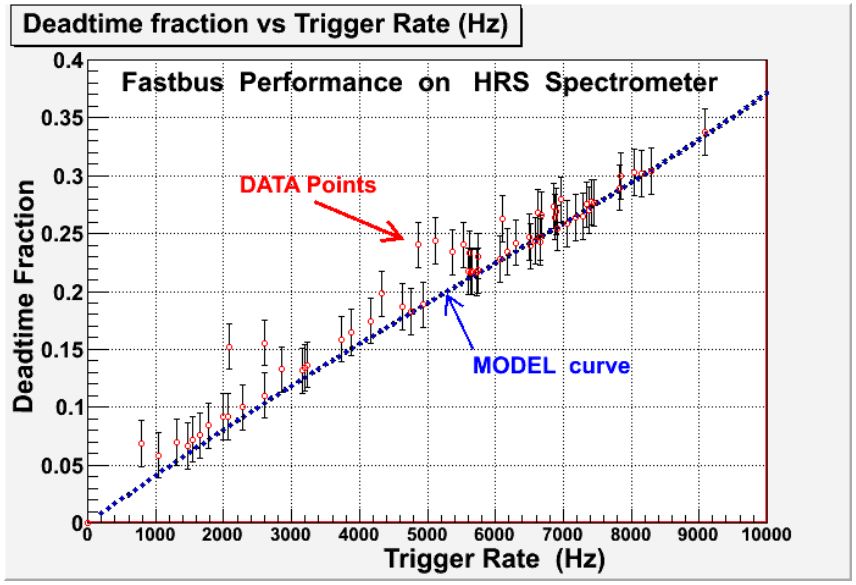
Status: tried, works

III. Event Switching

3 parallel crates reduces rate by 3



Status: test about to start



Based on **experience**

with Fastbus we can predict the performance of the

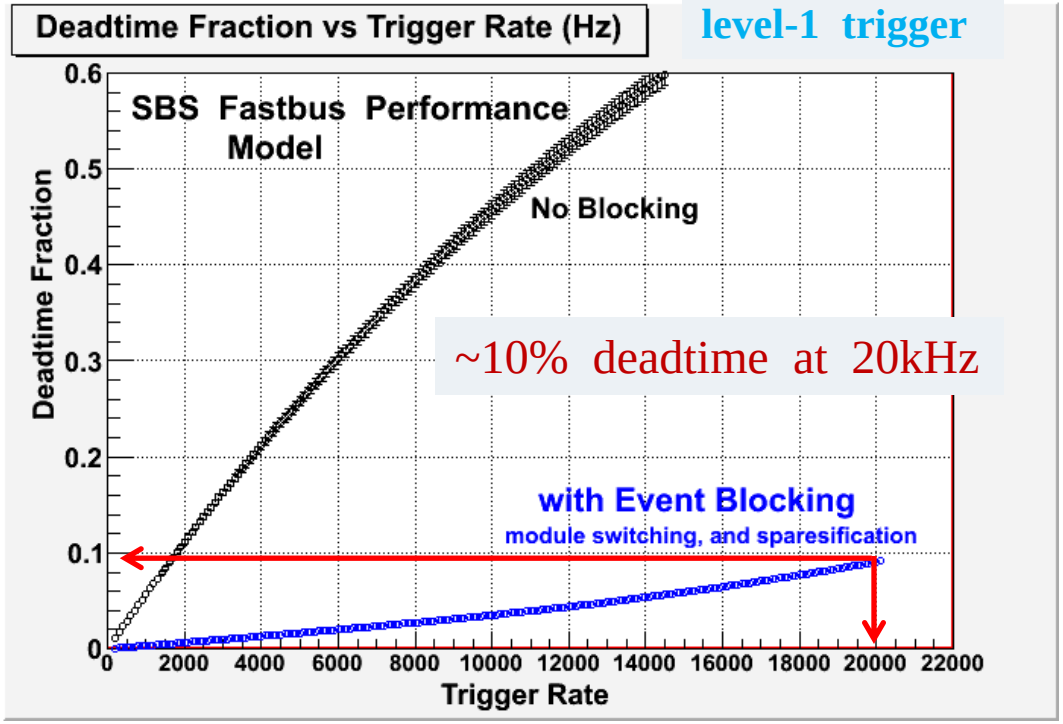
SBS Fastbus system

We can merge Fastbus with the rest of the DAQ if

- All components use blocklevel = 4
- All crates conform to the CODA standard.

This needs to be tested

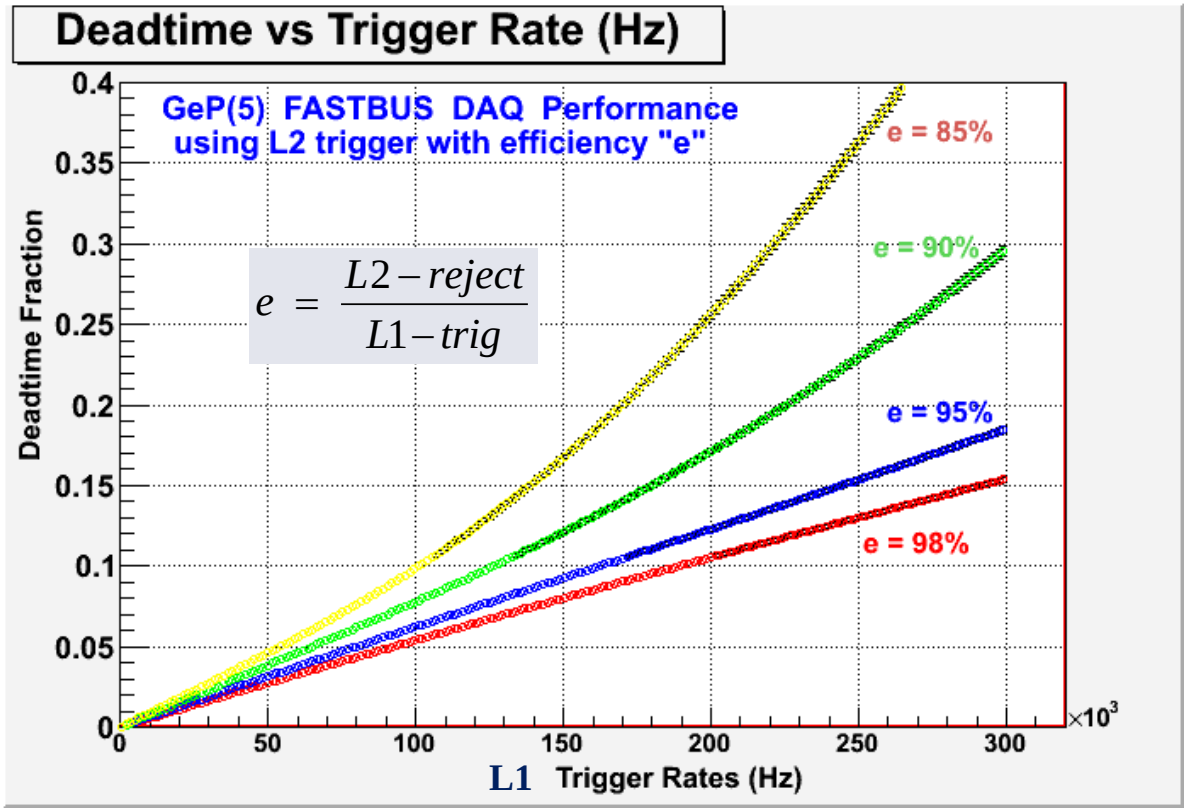
For a simple level-1 trigger



GeP(5) is the most demanding

For Fastbus, the plan is to use second-level (L2) triggers to issue a fast clear.

Singles L1 trigger rate 100 – 300 kHz depending on thresholds.
L2 rejection 80% or greater.



Fastbus Status

- Have sufficient TDCs, ADCs, crates, aux. cards

TDCs	ADCs	crates
have 236	have 113	have 30
need 124	need 94	need 21

- Like to scrounge ~3 more SFI (Struck Fastbus Interface)

  (have ~0 spare SFI; backup plan: reduced num crates, reduced performance)

- Making FB faster
  - sparsification – works
  - event blocking – works
  - event switching -- to be tried, looks feasible
  - merging with pipelining VME -- to be tried

- Two large fastbus systems are being assembled for test in the test lab.