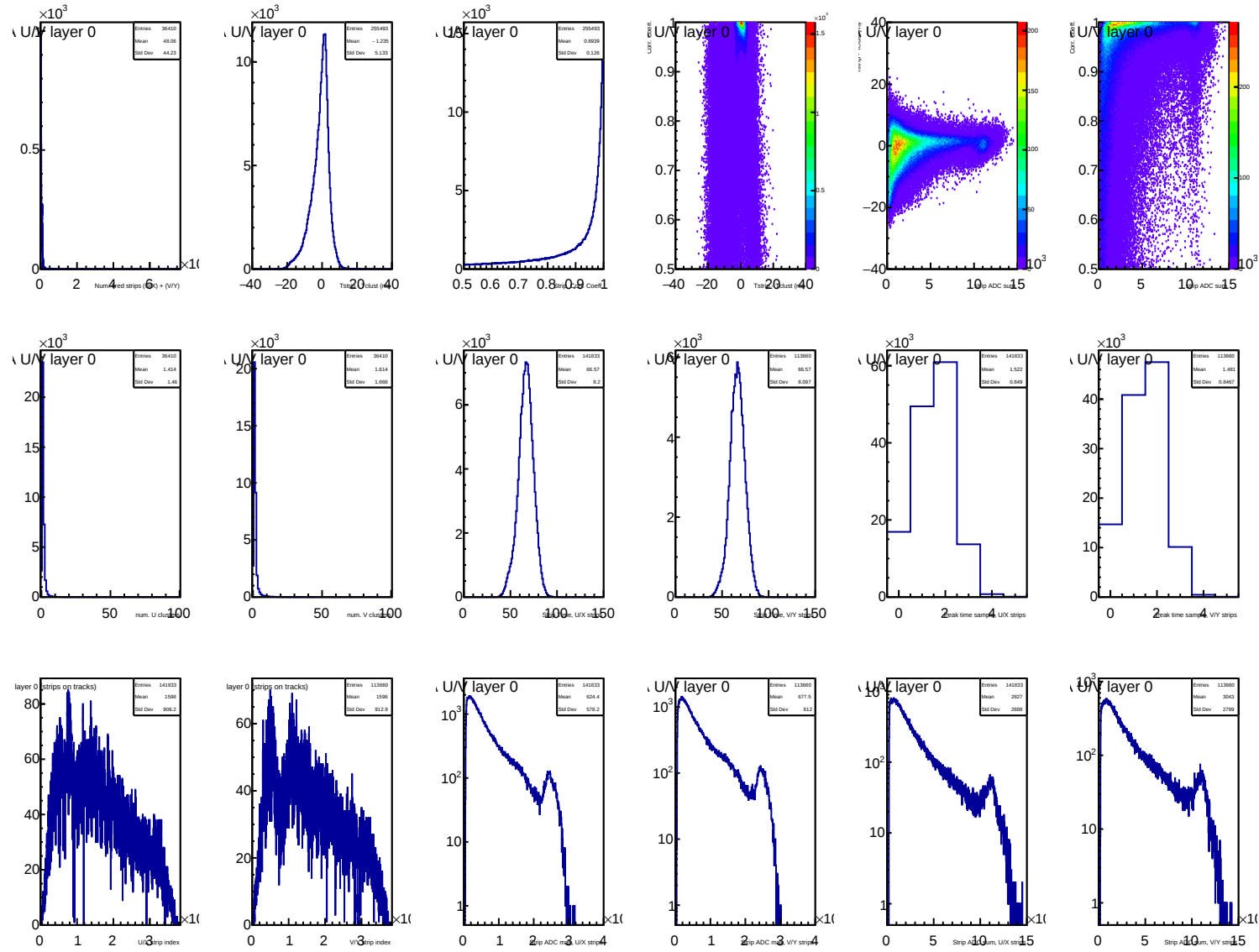
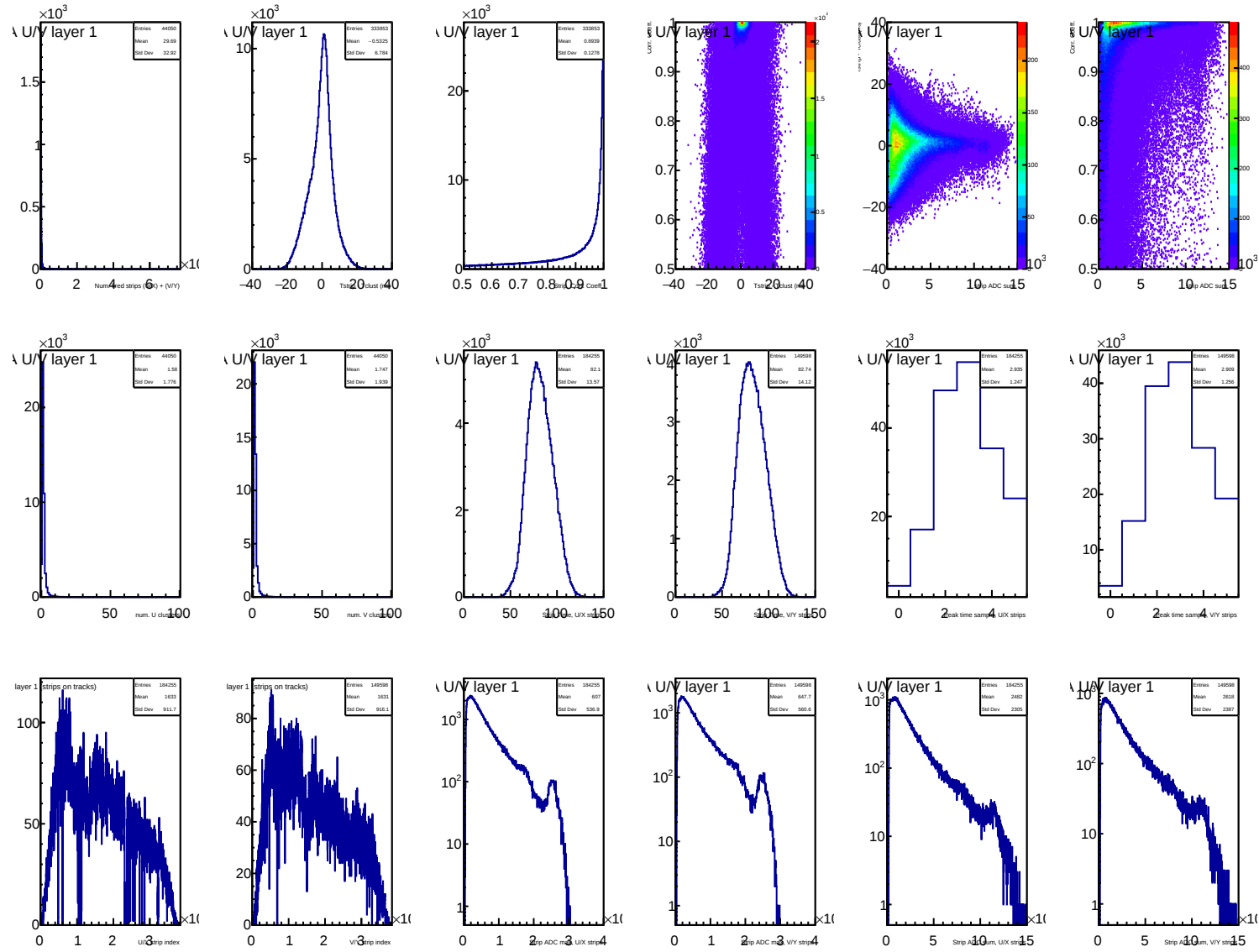


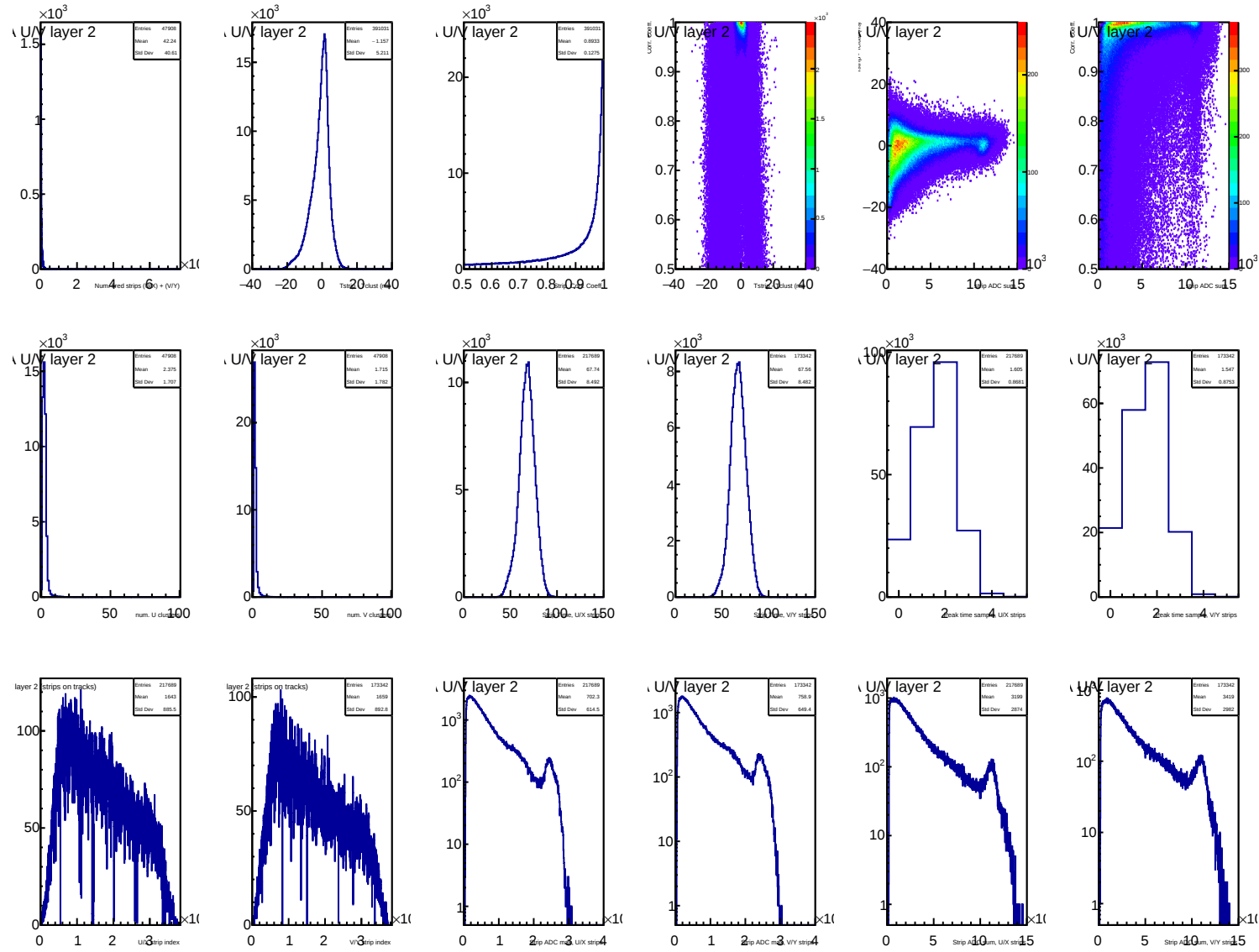
Summary Plots(Run #13286 0: UVA U/V layer 0 low-level (with track cuts)



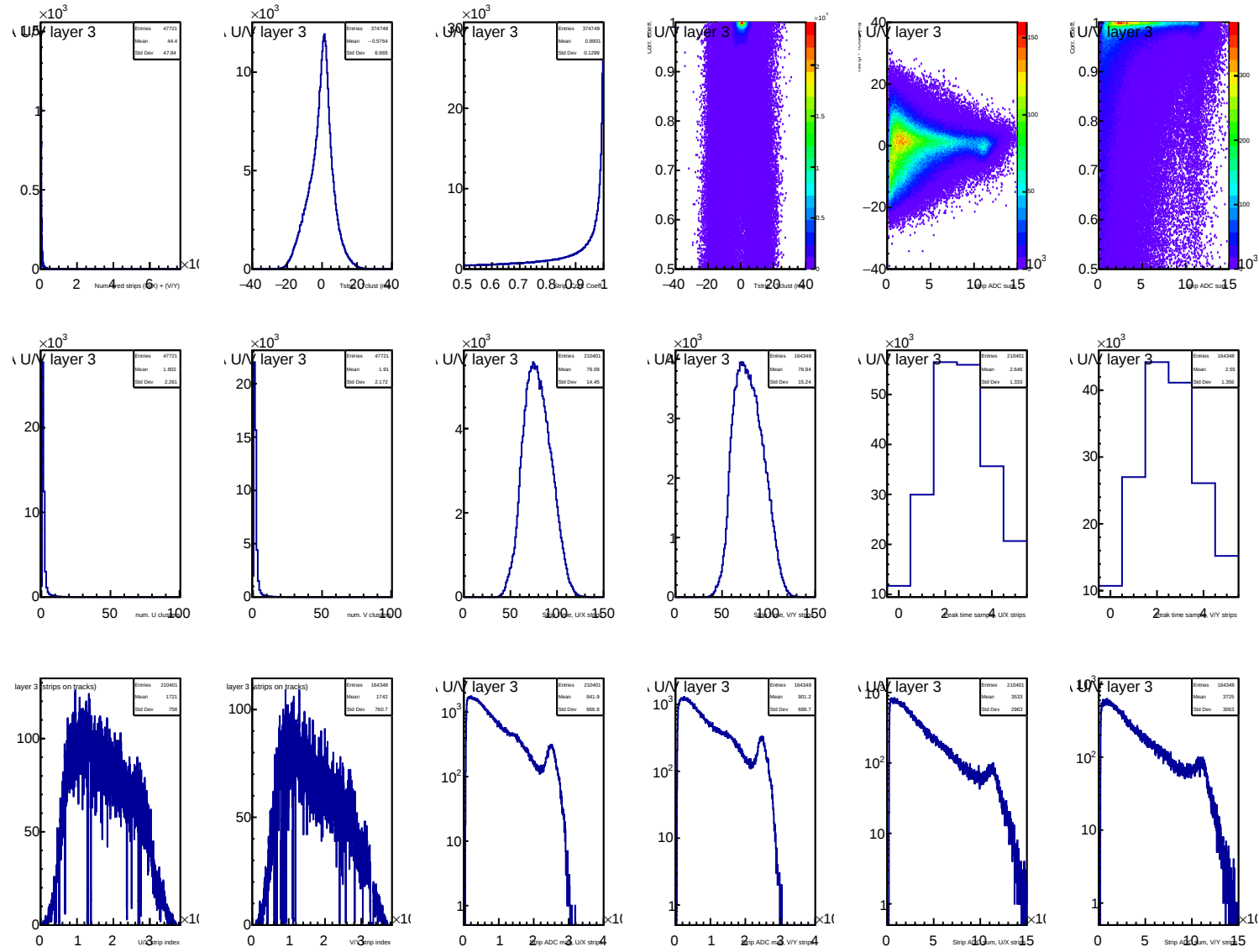
Summary Plots(Run #13286) 1: UVA U/V layer 1 low-level (with track cuts)



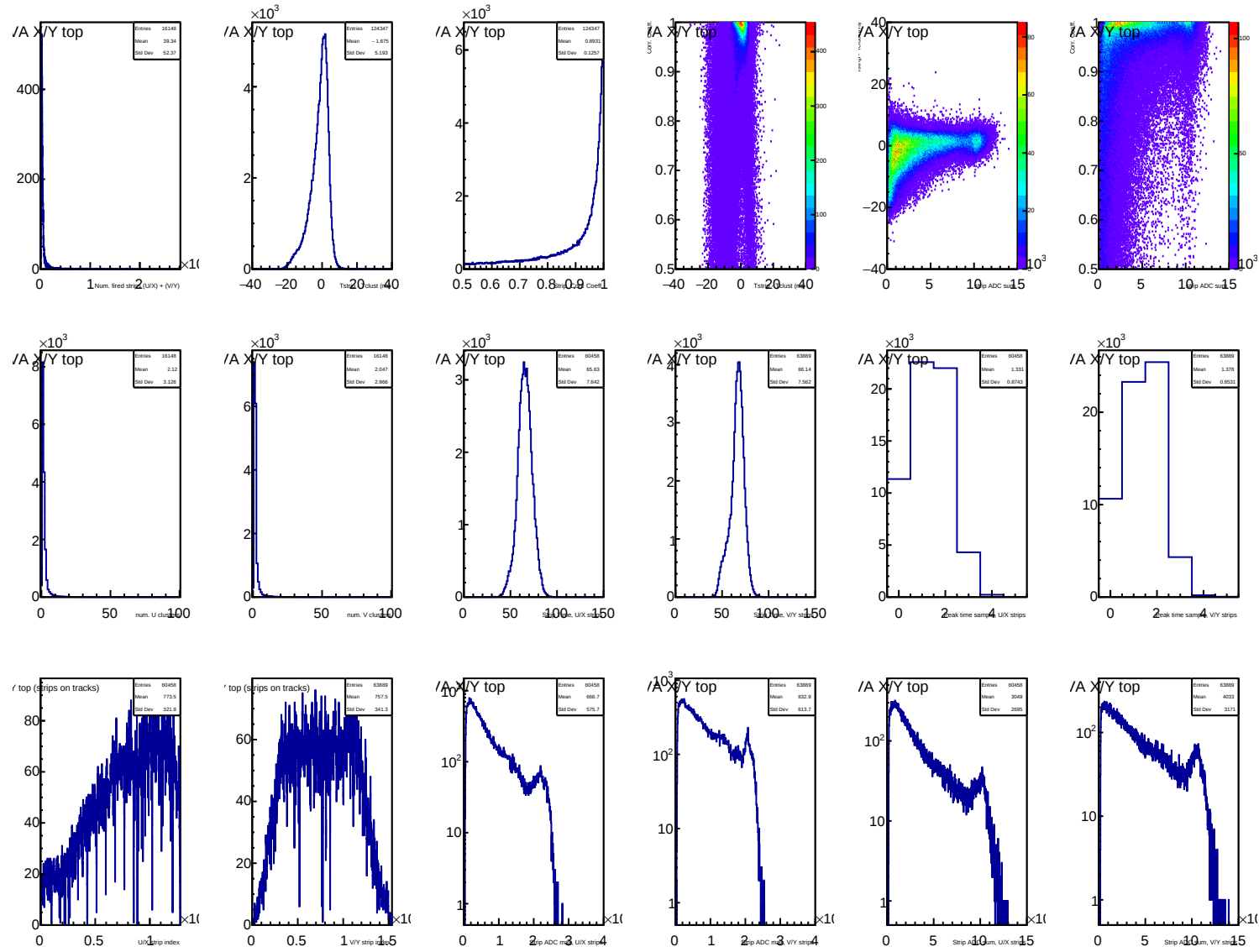
Summary Plots(Run #13286) 2: UVA U/V layer 2 low-level (with track cuts)



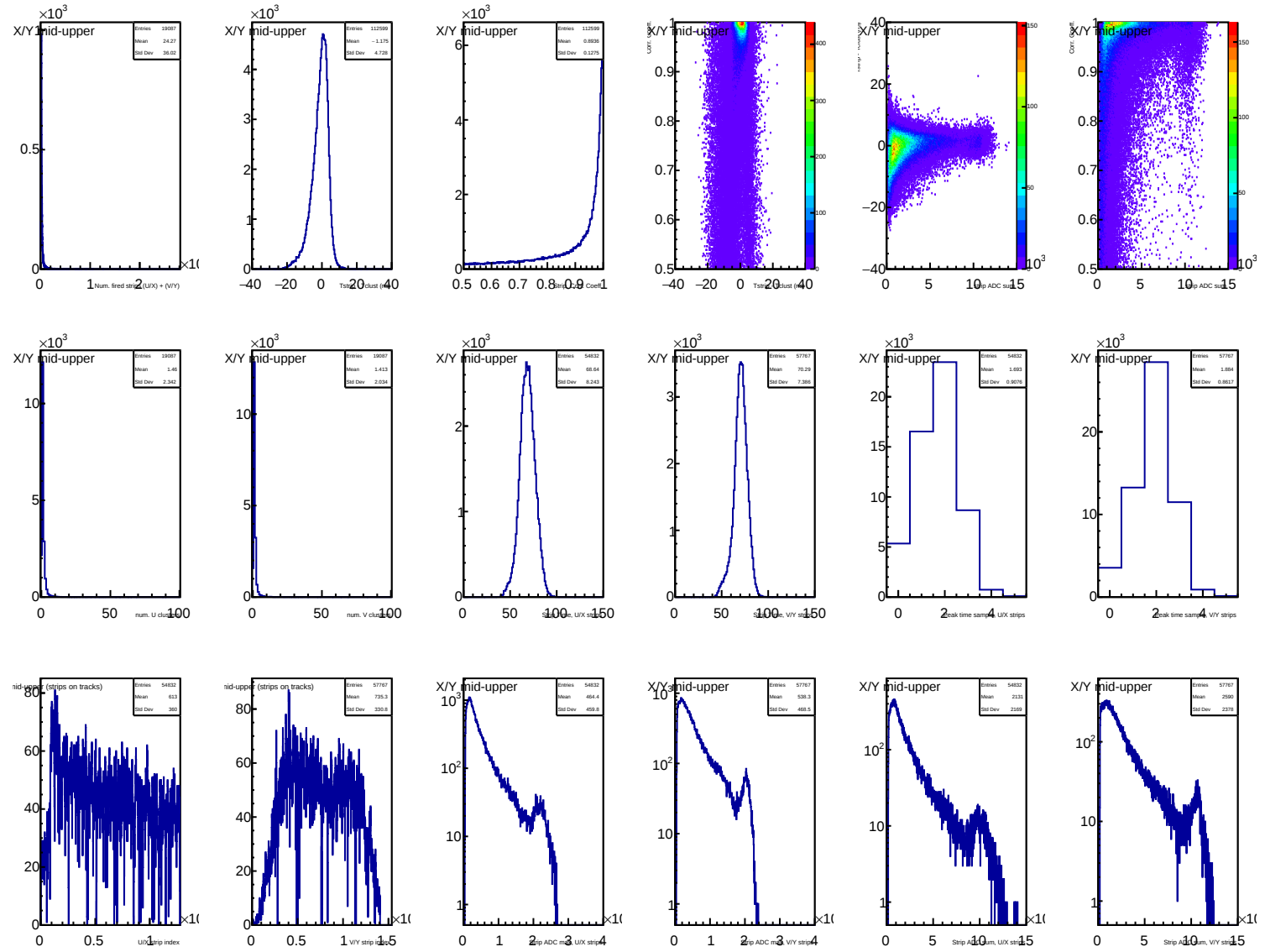
Summary Plots(Run #13286) 3: UVA U/V layer 3 low-level (with track cuts)



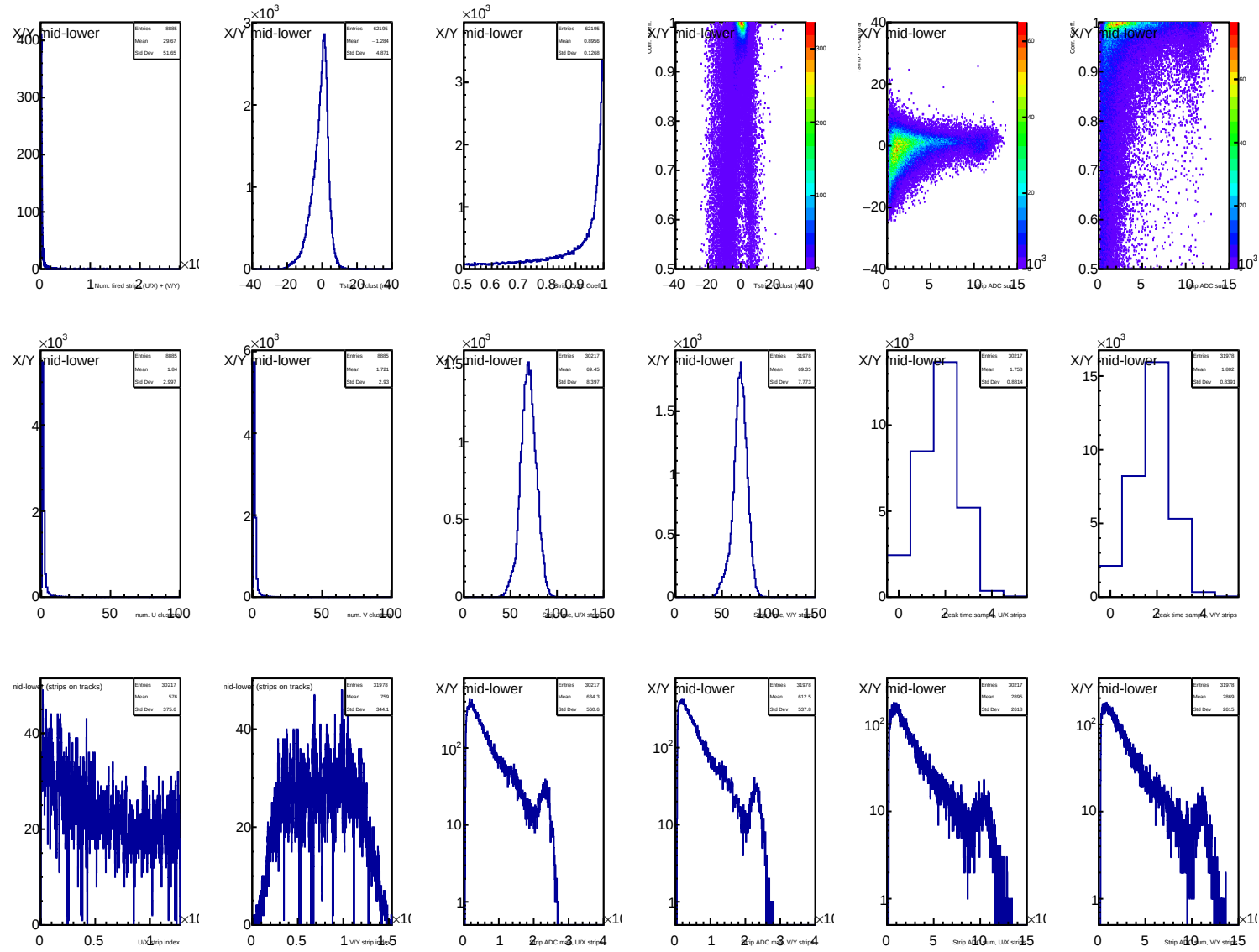
Summary Plots (Run #13286) 4: UVA X/Y top low-level (with track cuts)



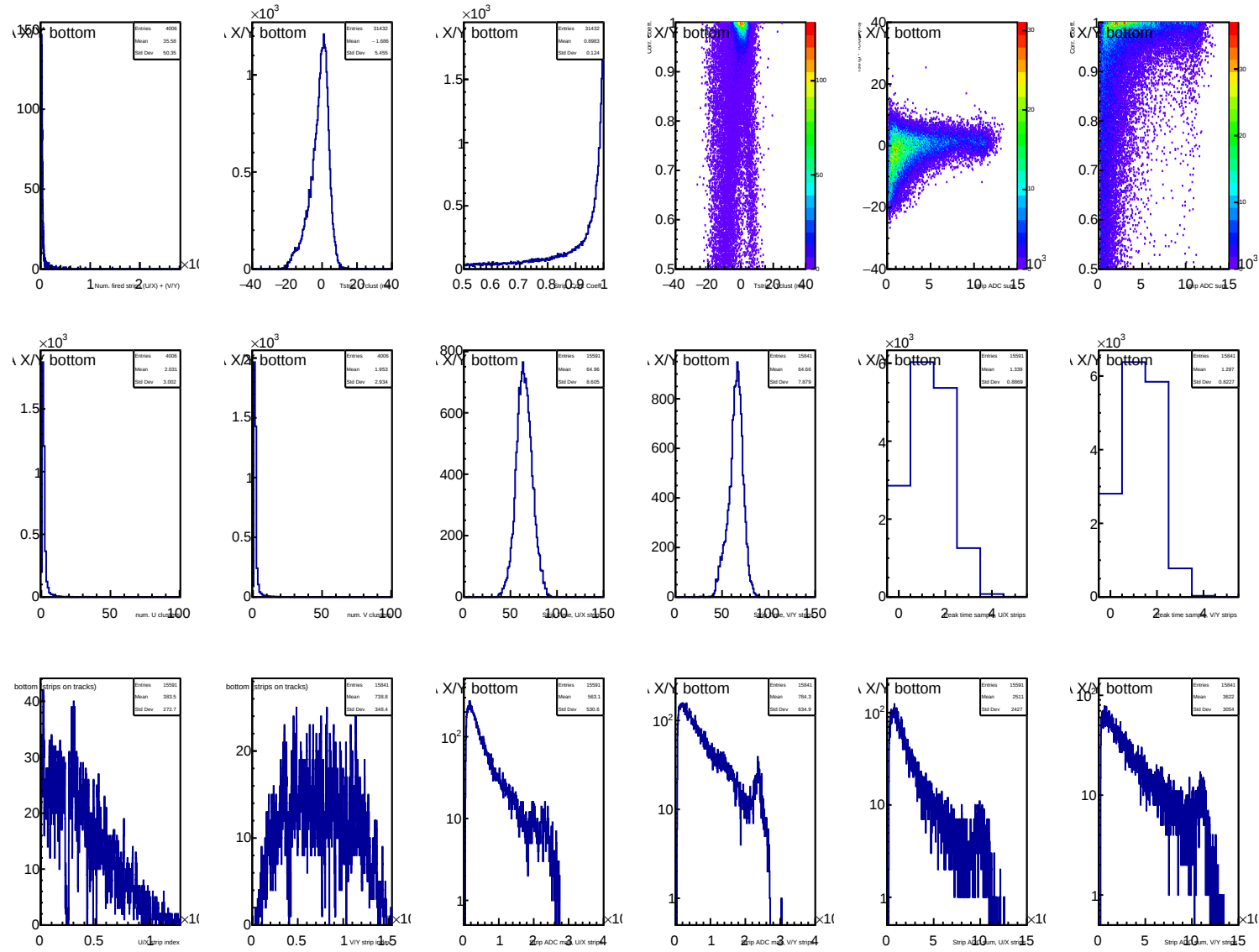
Summary Plots(Run #13286) 5: UVA X/Y mid-upper low-level (with track cuts)



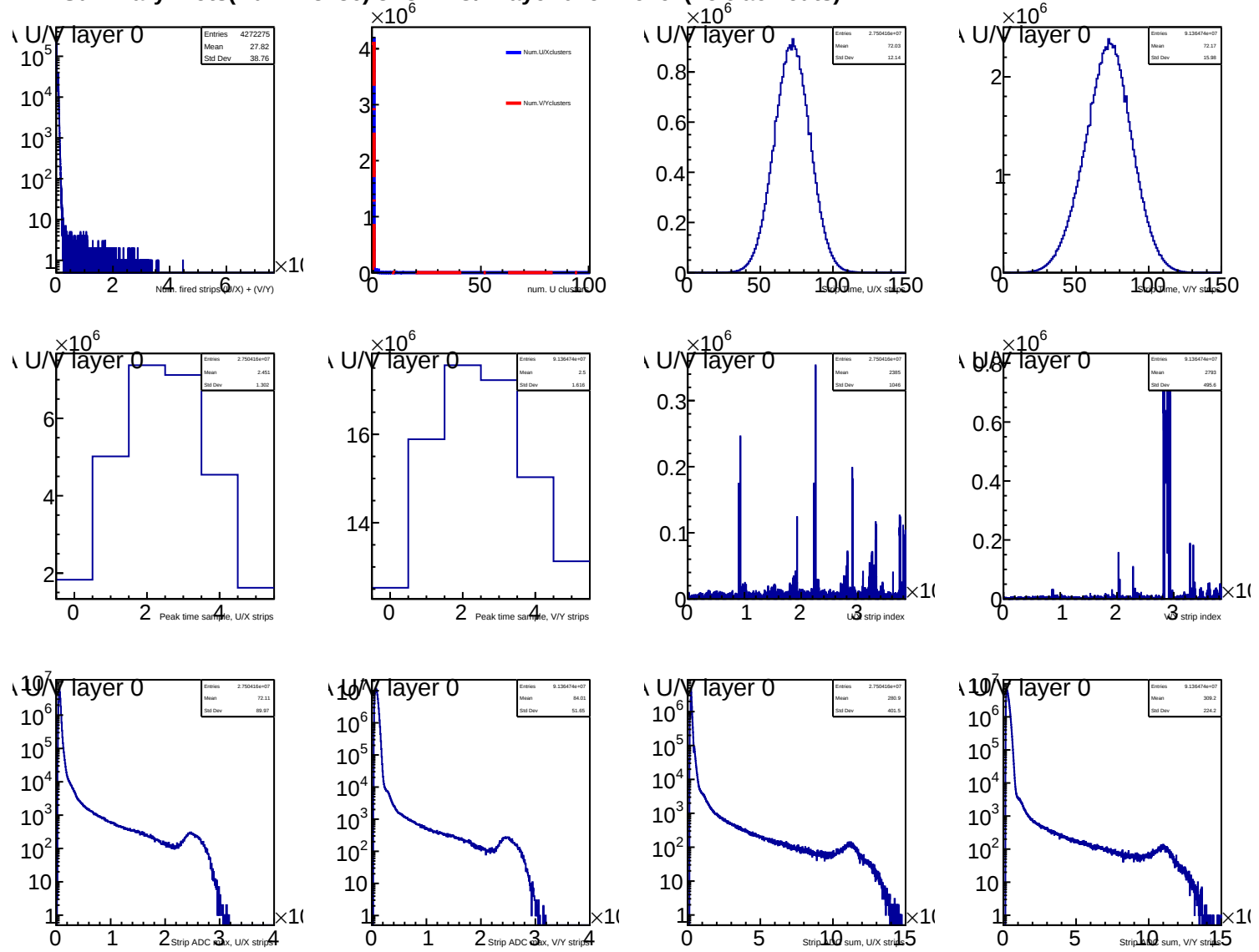
Summary Plots(Run #13286) 6: UVA X/Y mid-lower low-level (with track cuts)



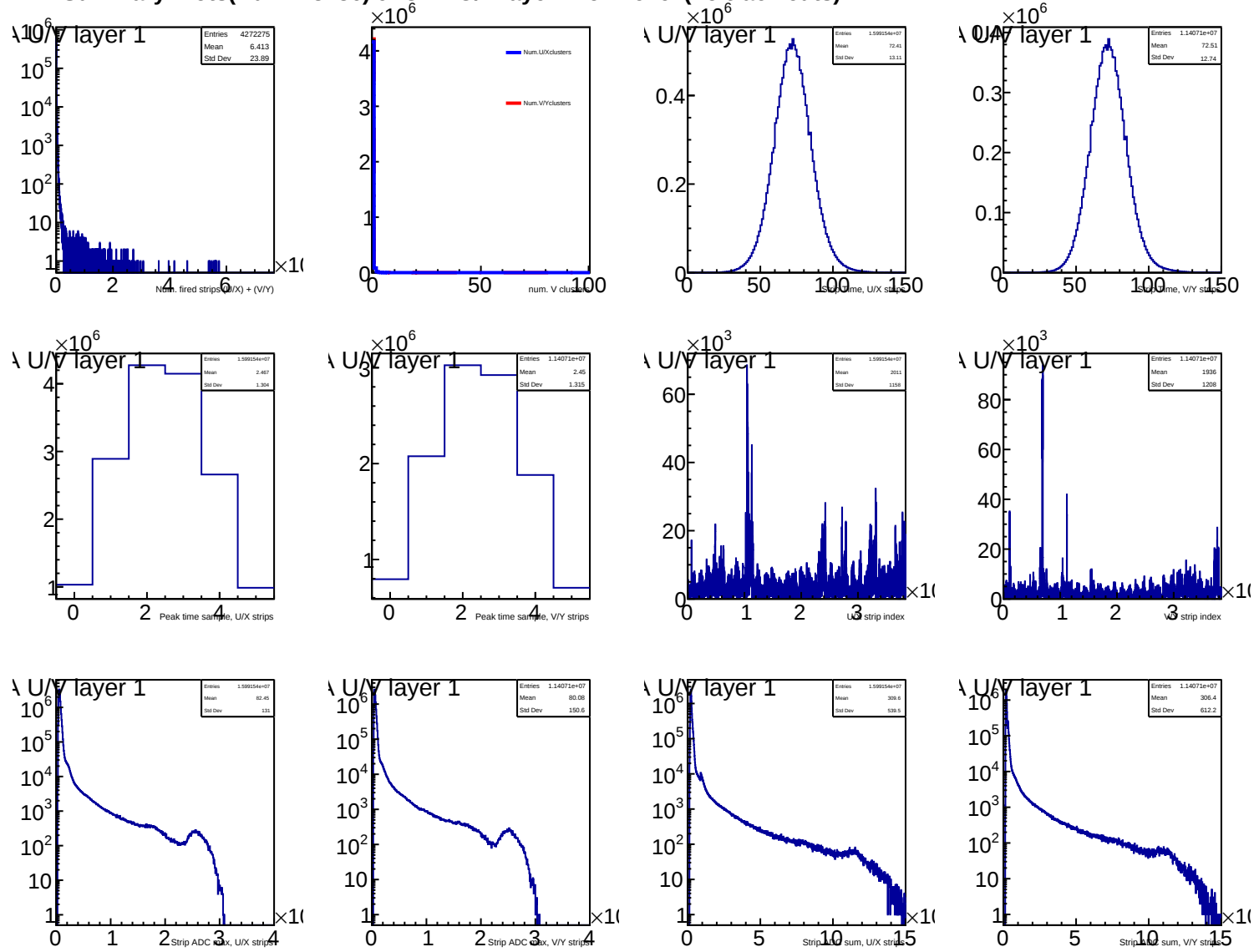
Summary Plots(Run #13286) 7: UVA X/Y bottom low-level (with track cuts)



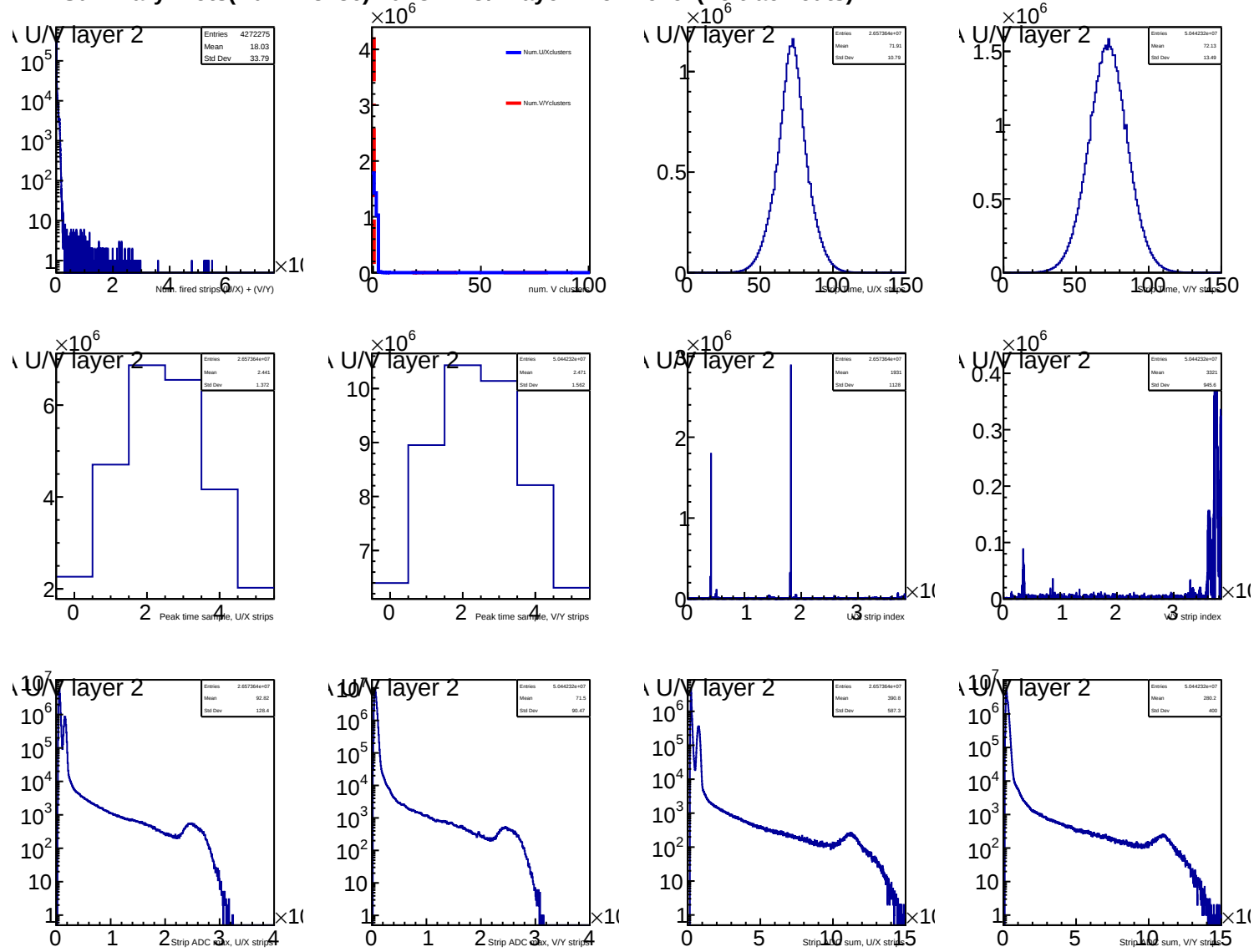
Summary Plots(Run #13286) 8: UVA U/V layer 0 low-level (no track cuts)



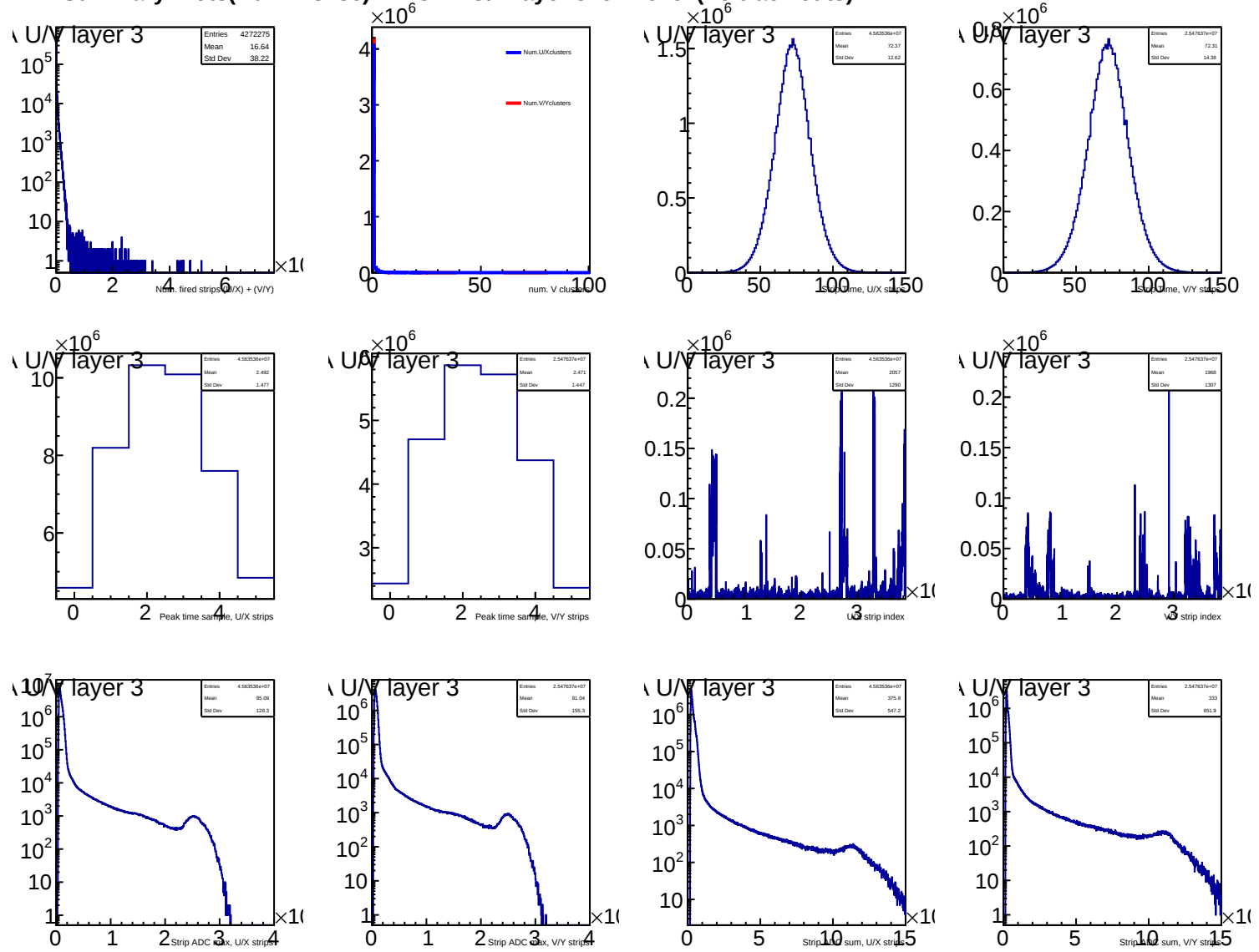
Summary Plots(Run #13286) 9: UVA U/V layer 1 low-level (no track cuts)



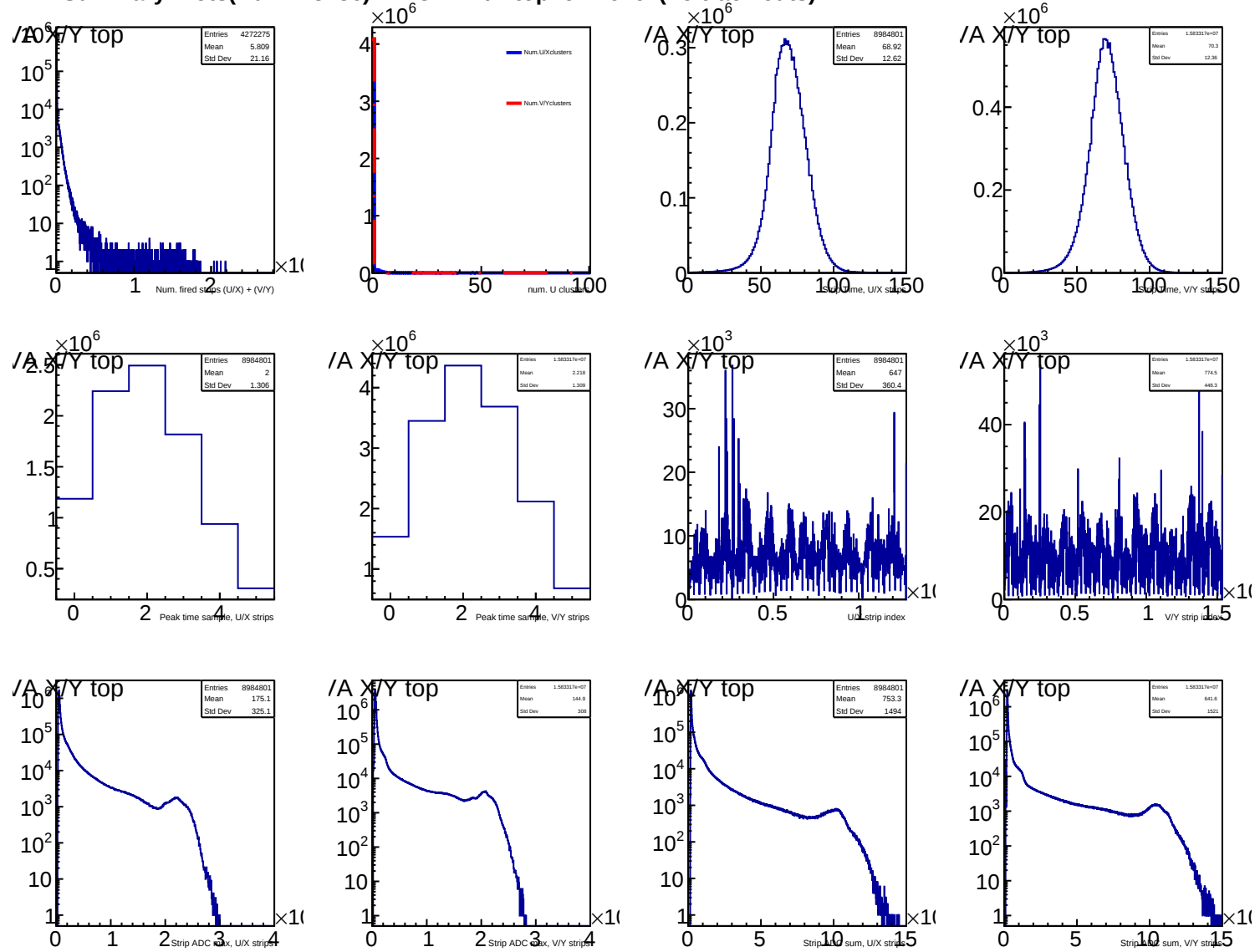
Summary Plots(Run #13286) 10: UVA U/V layer 2 low-level (no track cuts)



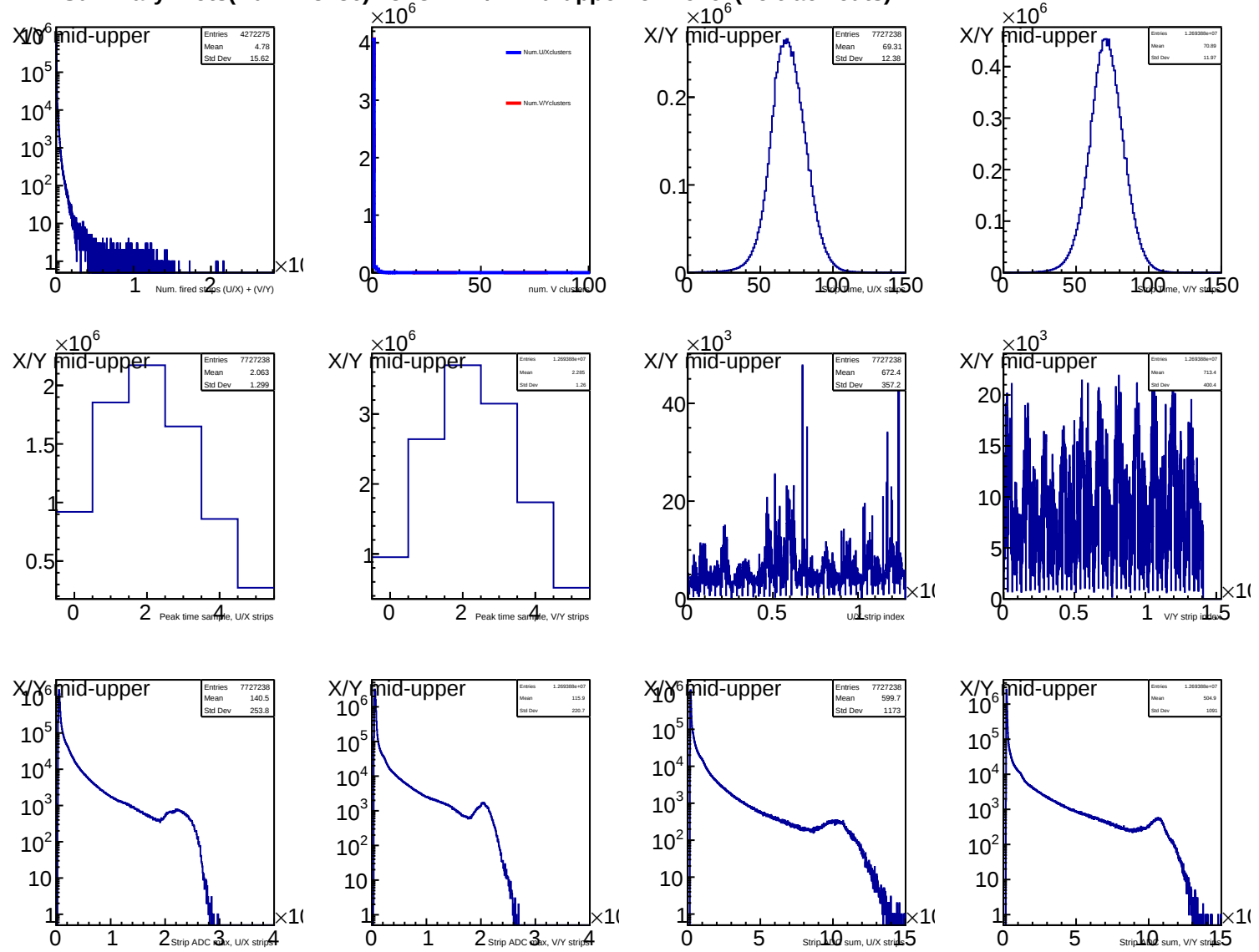
Summary Plots(Run #13286) 11: UVA U/V layer 3 low-level (no track cuts)



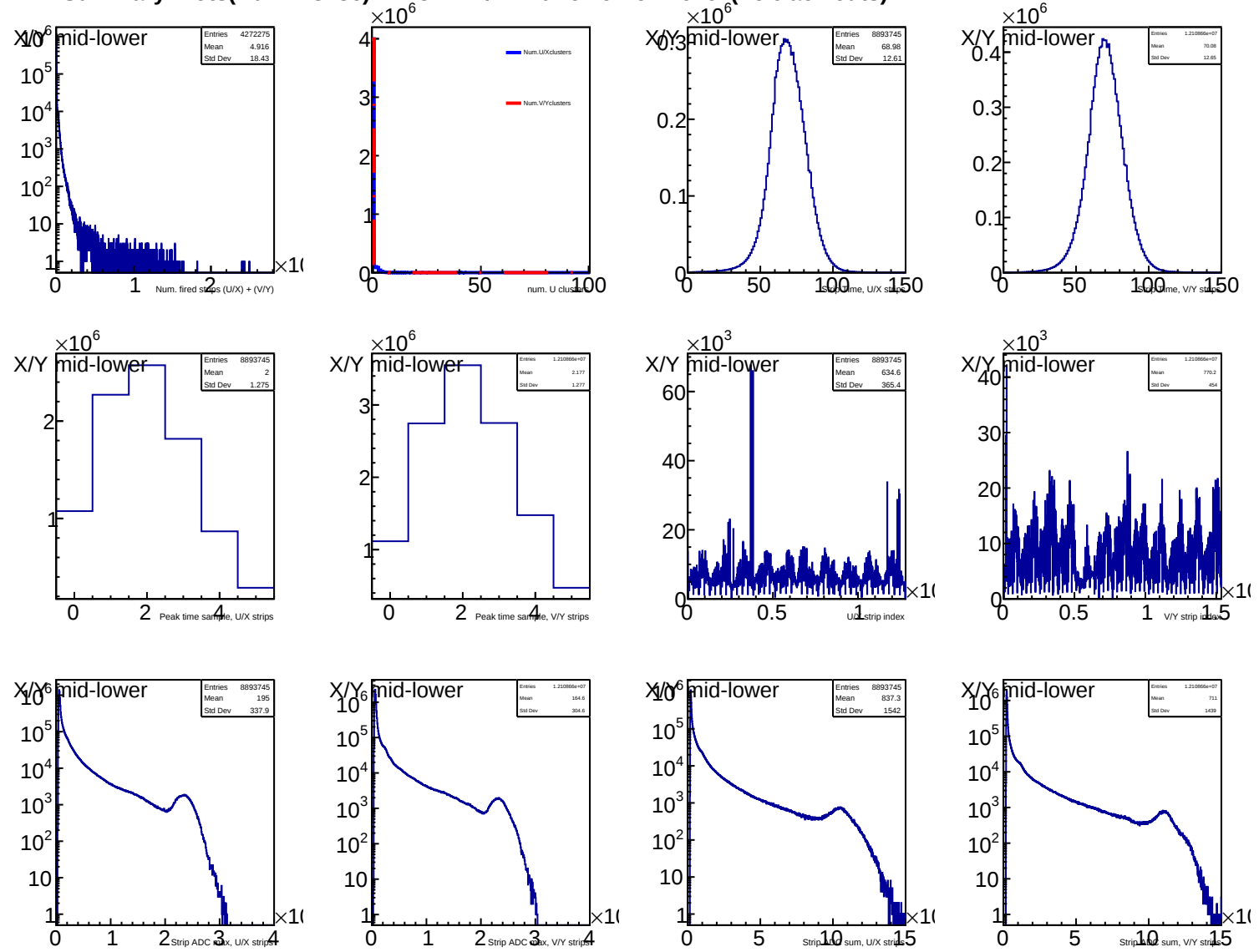
Summary Plots(Run #13286) 12: UVA X/Y top low-level (no track cuts)



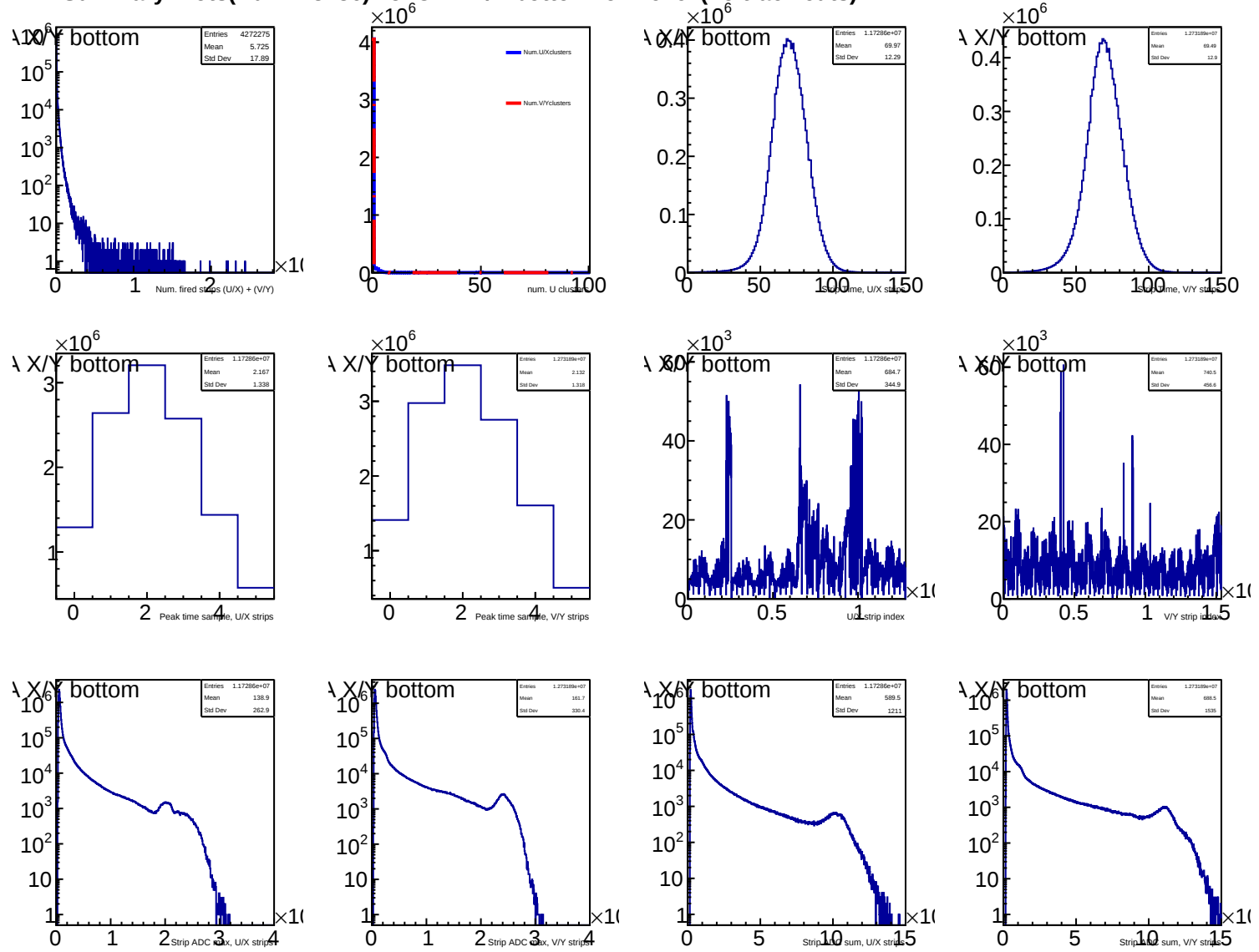
Summary Plots(Run #13286) 13: UVA X/Y mid-upper low-level (no track cuts)



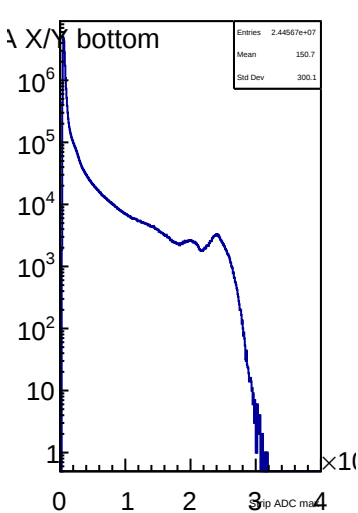
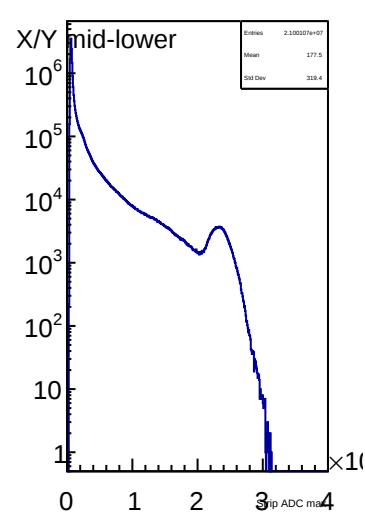
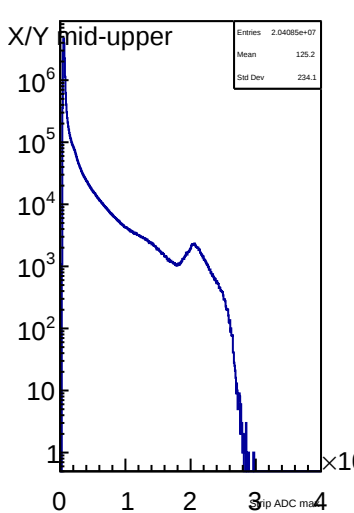
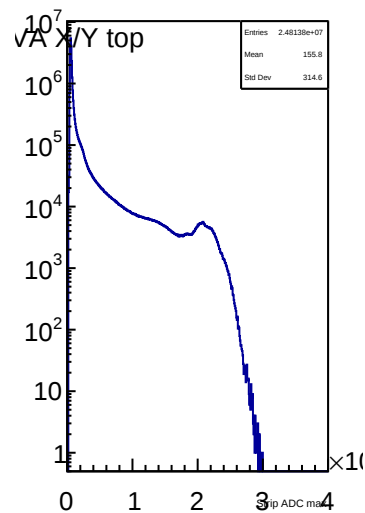
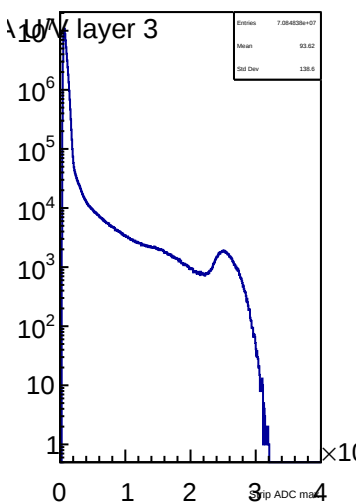
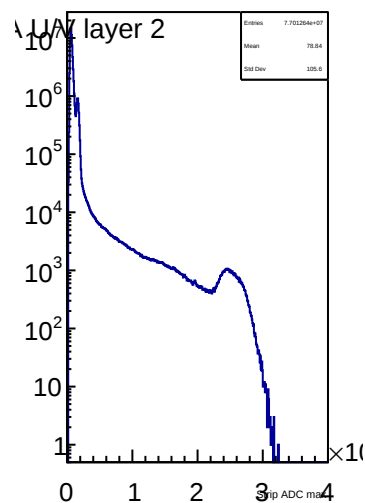
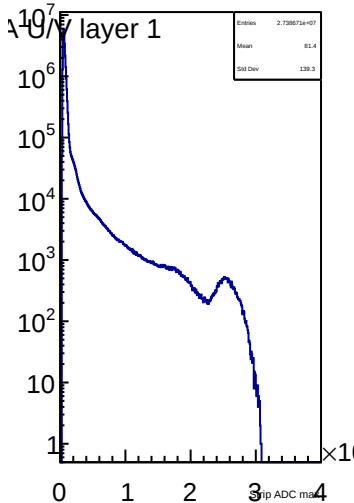
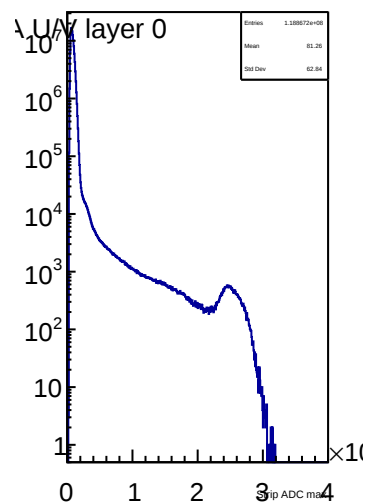
Summary Plots(Run #13286) 14: UVA X/Y mid-level low-level (no track cuts)



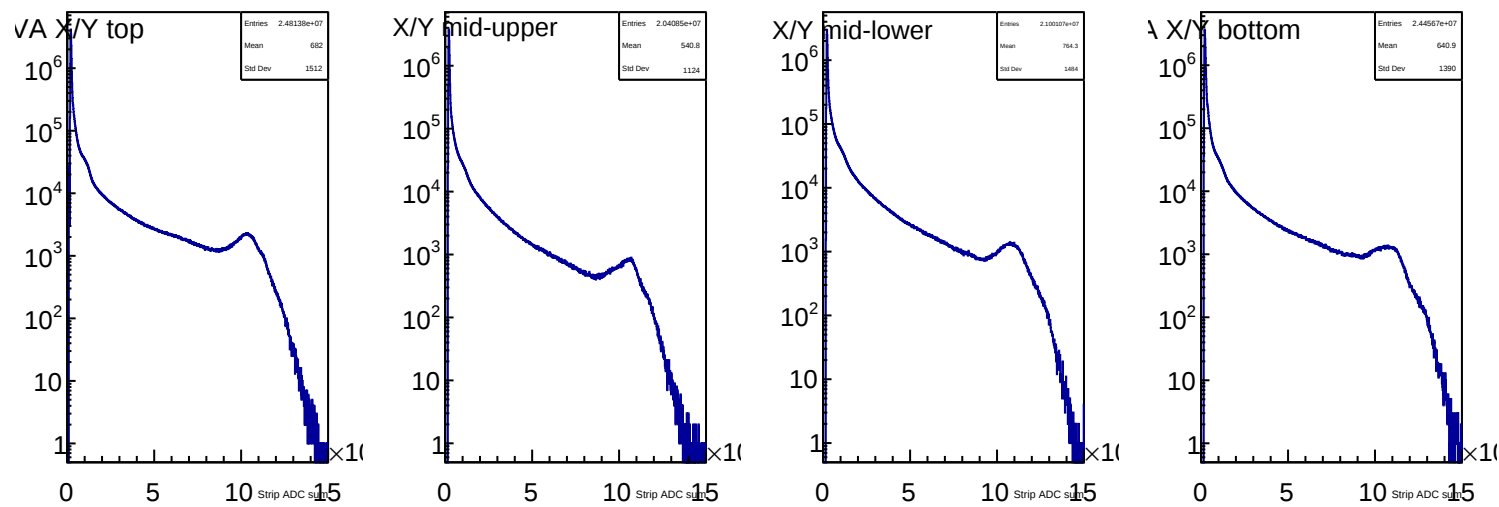
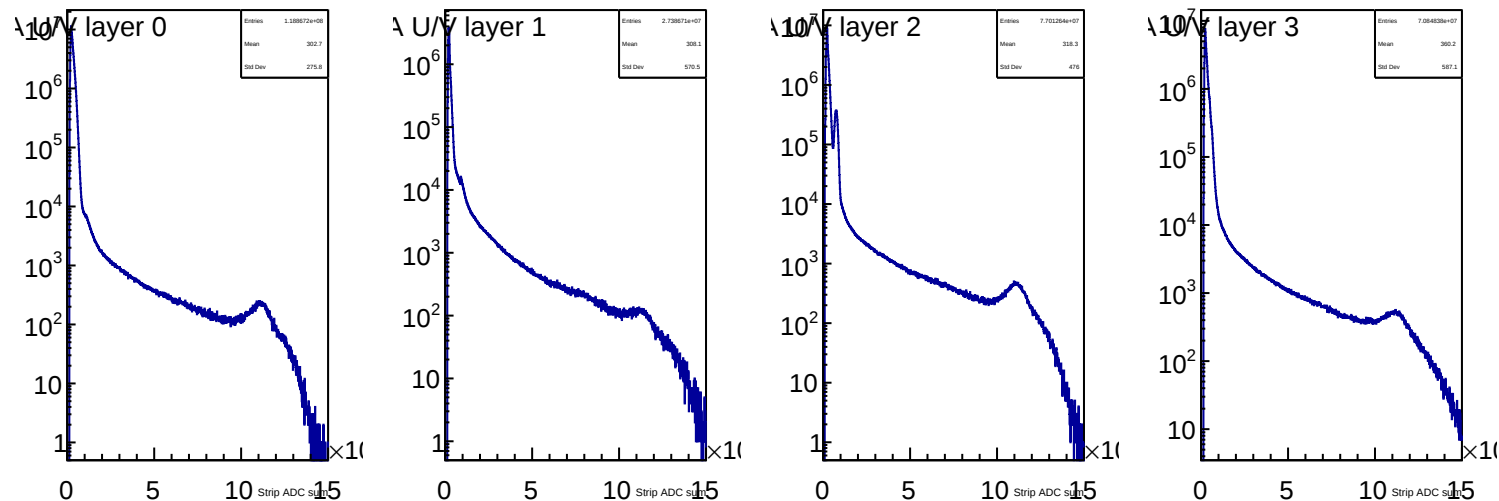
Summary Plots(Run #13286) 15: UVA X/Y bottom low-level (no track cuts)



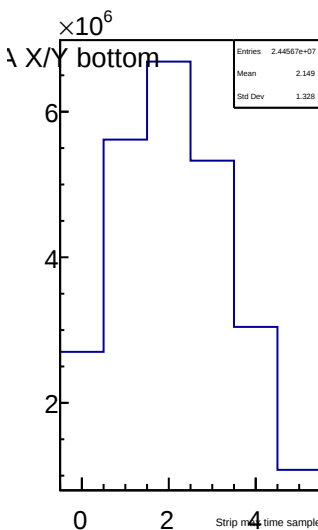
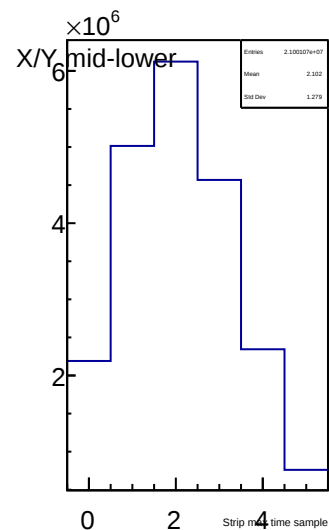
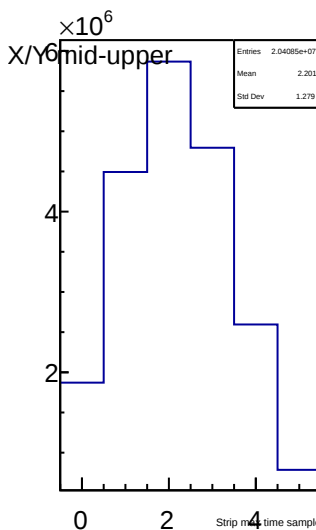
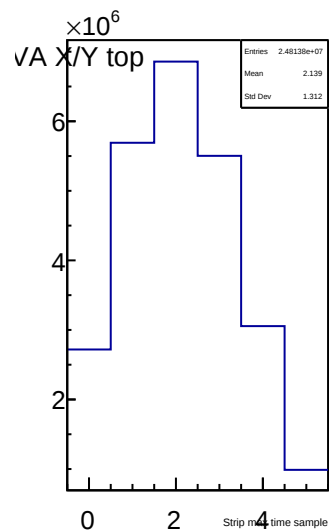
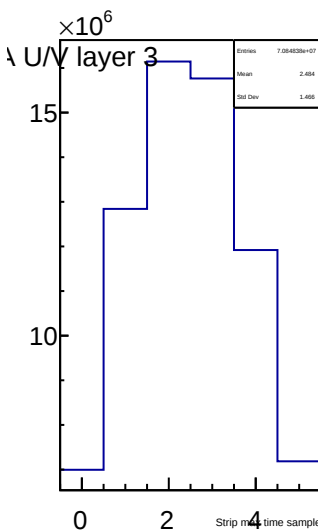
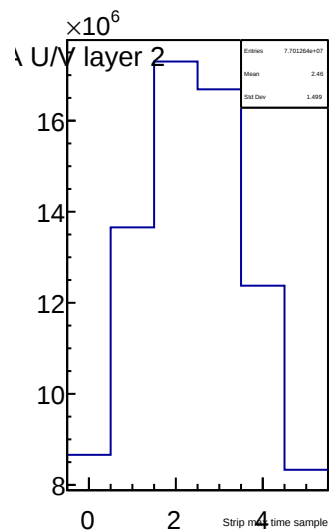
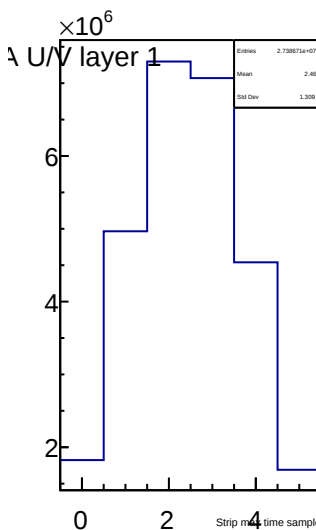
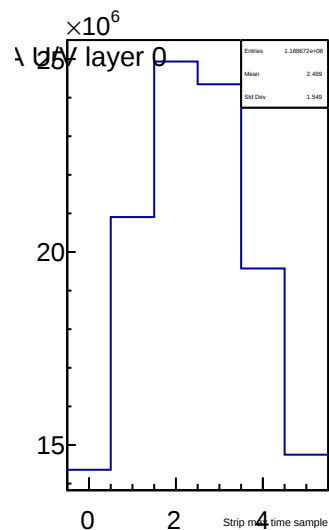
Summary Plots(Run #13286) 16: All modules strip ADC max



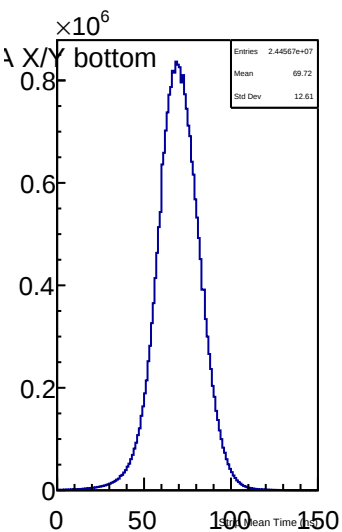
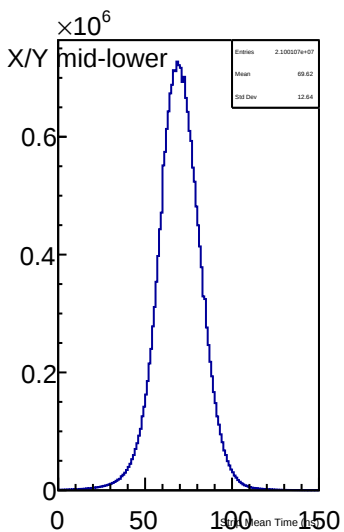
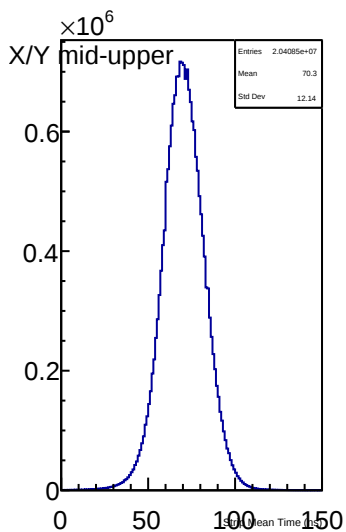
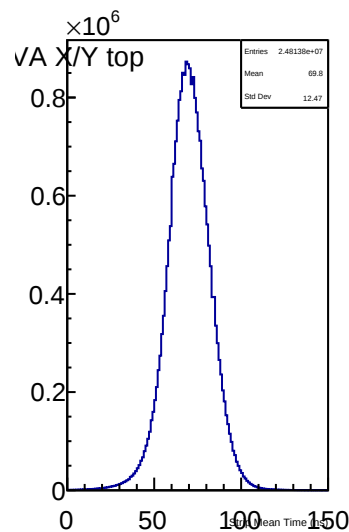
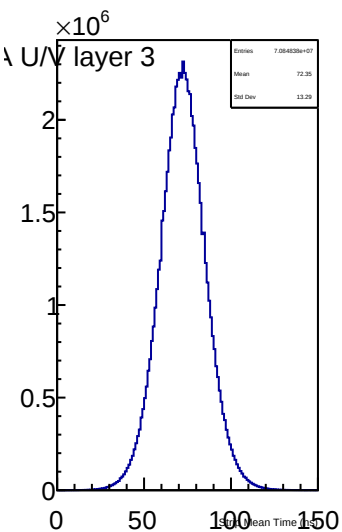
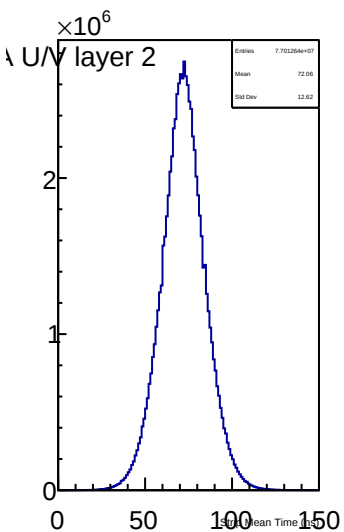
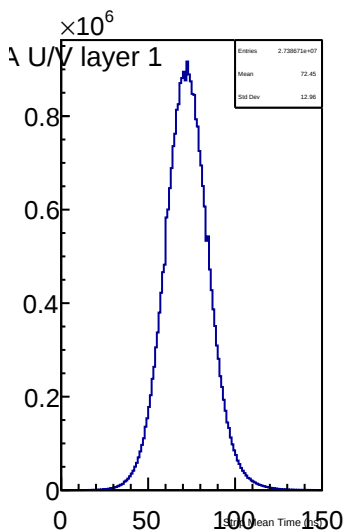
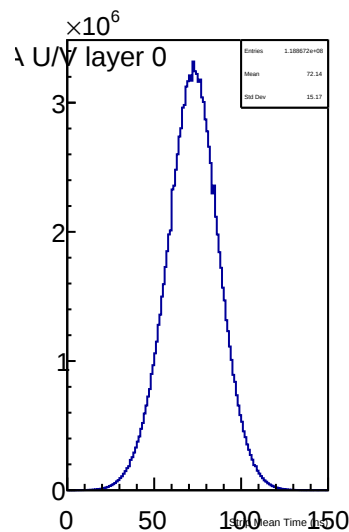
Summary Plots(Run #13286) 17: All modules strip ADC sum



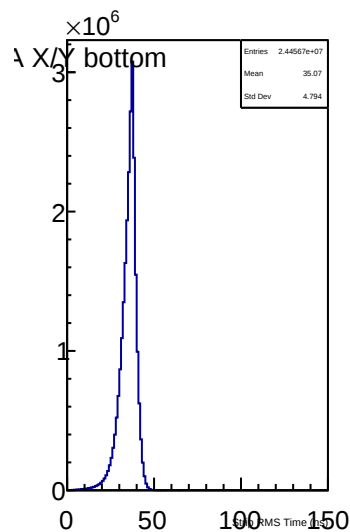
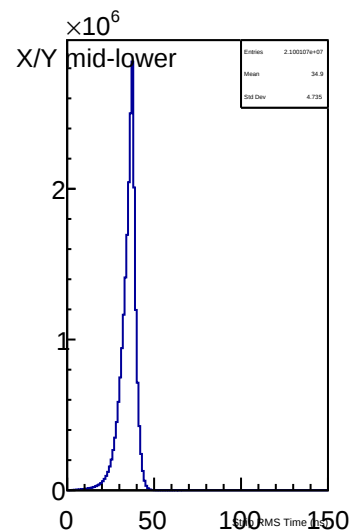
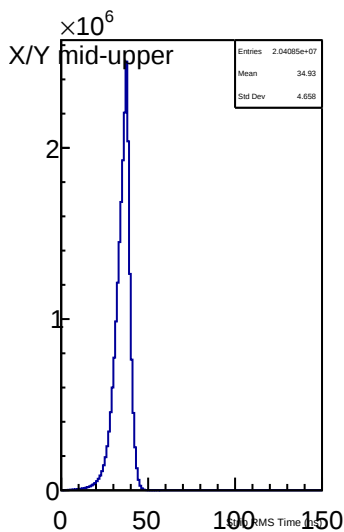
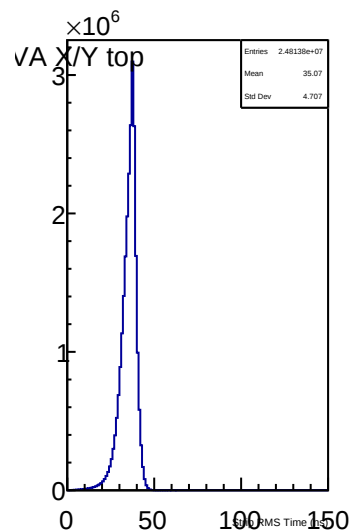
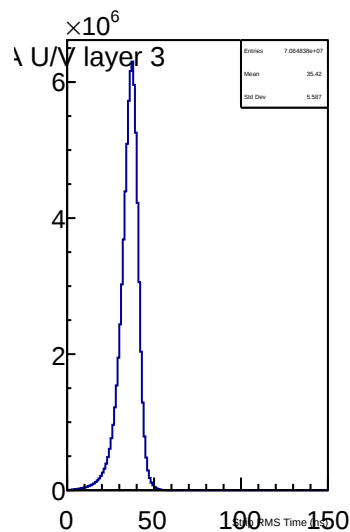
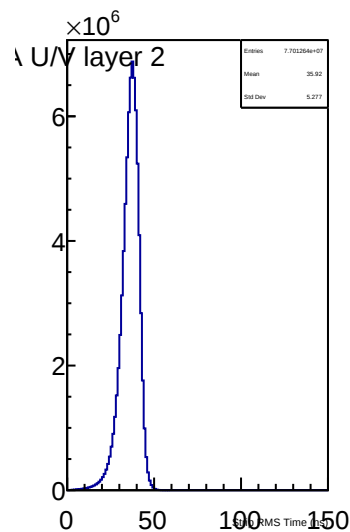
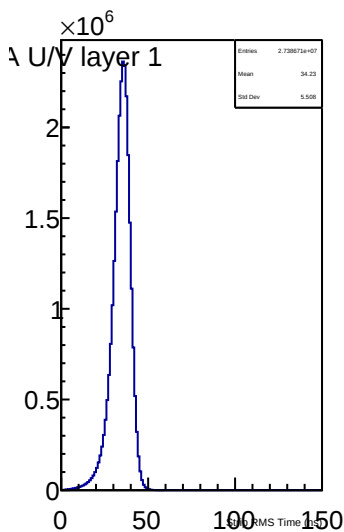
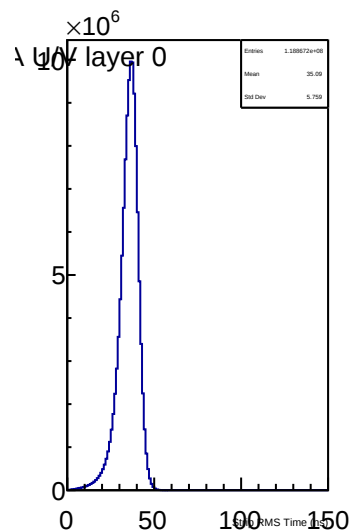
Summary Plots(Run #13286) 18: All modules max time sample



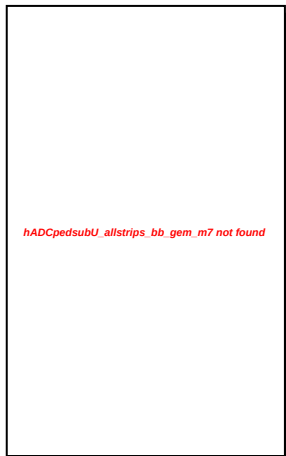
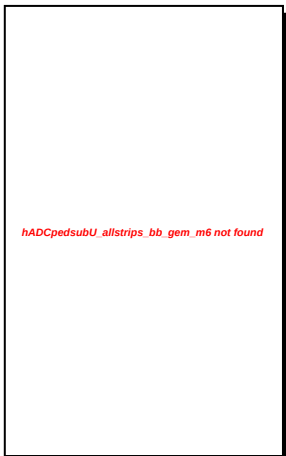
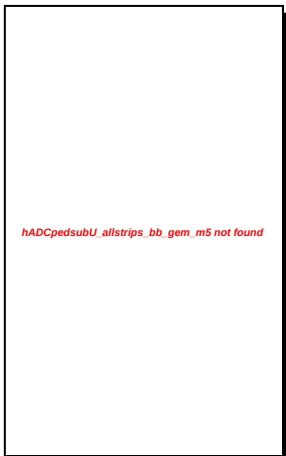
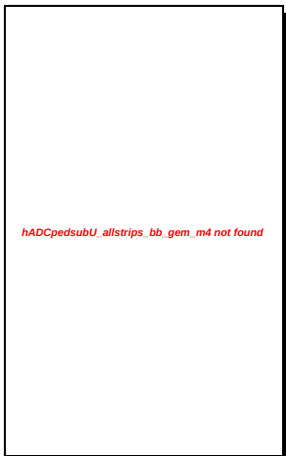
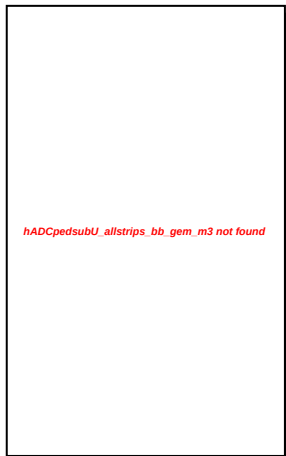
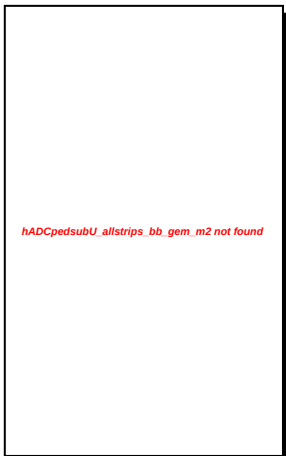
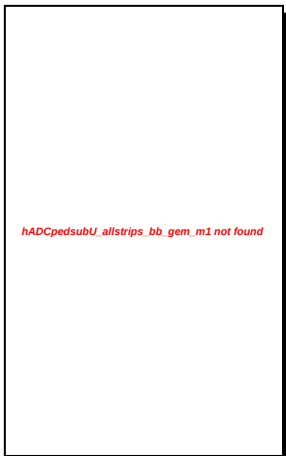
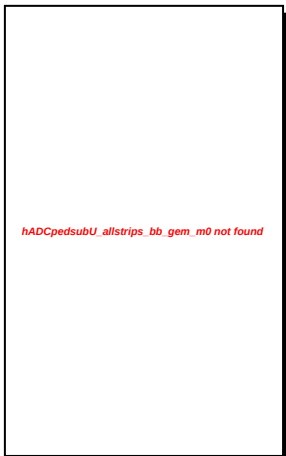
Summary Plots(Run #13286) 19: All modules strip time



Summary Plots(Run #13286) 20: All modules strip rms time



Summary Plots(Run #13286) 21: All modules U strip ADC no zero sup



Summary Plots(Run #13286) 22: All modules V strip ADC no zero sup

