# A Novel Modular and Flexible Readout Electronics for Photon Imaging Applications

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***Abstract*–The design and first test results of new readout electronics for a Multi Anode PhotoMultiplier Tube (MAPMT) array is reported. The system has been developed to perform the readout of arrays of 64 or 256-channels MAPMTs, used in single photon imaging applications, such as Single Photon Emission Computed Tomography (SPECT) for medical studies on stem cells or clinical diagnosis of breast-cancer.**

**The electronics features good compactness and modularity. It is organized according to a hierarchical architecture, based on extensive use of Field Programmable Gate Arrays (FPGA).**

**The system is built around the MAROC2, a VLSI 64-channel front-end chip, with self-triggering capability and multiplexed output of independent channels. The basic building block is the small Front-End card (FE) which accommodates a MAROC2 device and an FPGA in charge of configuring the front-end chip and handling the readout modes. The FE cards communicate with the Control Board (CB), also FPGA-based, by means of the Backplane (BP) card, using a custom protocol which implements an event-driven readout. Among the other tasks, the CB card manages the USB 2.0 communication with a PC.**

**By design the system can readout up to 4096 channels and sustains an event rate of 30 KHz, with a 12 bit resolution in A/D conversion.**

**The features of the proposed readout electronics make it especially suitable for other applications, such as imagers in Ring Imaging Cherenkov (RICH) detectors. The readout of other detectors, such as Silicon PhotoMultiplier (SiPM), is also possible with a straightforward upgrade of the system.**

## I. Introduction

We propose a novel readout electronics for arrays of Multi Anode PhotoMultiplier Tubes (MAPMT), Flat Panel PMTs or, potentially, Silicon PhotoMultipliers.

The system has been designed to be well suitable for gamma photon imaging applications such as gamma camera for Single Photon Emission Computed Tomography (SPECT) or imager in Ring Imaging Cherenkov (RICH) detectors. In particular the development has been driven by specific requirements of a compact gamma camera for SPECT using an array of Flat Panel PMTs with 64 or 256 channels each.

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SPECT is a nuclear molecular imaging technique for non invasive, early disease diagnosis and in vivo studies of human diseases development and therapeutic response in small animal model [1].

Such a gamma camera features small size and reduced costs compared to a camera for traditional Positron Emission Tomography and consists of:

- a single/multi pin hole or parallel hole collimator;
- a scintillator crystal for gamma to optical light conversion;
- array of MAPMTs for detection of the optical photons coming from the scintillator;
- the readout electronics;
- acquisition and image reconstruction software.

The electronics described in the document shows good compactness, high modularity, and flexibility thanks to extensive use of Field Programmable Gate Arrays (FPGA). The adopted solutions, which include self-triggering capability, allow to obtain an efficient event selection, and a very good acquisition rate.

Moreover the intrinsic in-system reconfiguration functionality of the FPGAs gives the possibility to implement different event selection algorithms and to adapt the system to application requirements.

The electronics has been tested both in laboratory and in the Test Beam Facility of INFN-LNF in Frascati (Rome, Italy), where it is used as imager for a prototype focusing Aerogel RICH.

## II. System Architecture

The electronics structure is organized according to a hierarchical scheme with a single main board, the Controller Board (CB), and several daughter boards, the Front-End boards (FE). The number of FEs depends on the number of pixel (anodes) to be readout: one FE is associated to 64 pixel channels. In the full configuration the system can perform the readout of 4096 channels i.e. 64 FE cards. The CB and FEs are connected by means of the BackPlane boards (BP) which give the mechanical support to the FEs and provide electrical connectivity.

A schematic of the electronics structure is presented in Fig. 1.

The chosen MAPMT target is the Hamamatsu H9500[2], a 256 anodes Flat Panel PMT. Four FE cards are needed for a H9500 and can be directly connected to it (Fig. 1), reducing parasitic coupling and ensuring good signal integrity.

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Up to 16 FE boards can be plugged in a single Backplane card, therefore 4 H9500 can be placed side by side with minimal dead area, resulting in a compact and complete building block of 1024 channels.

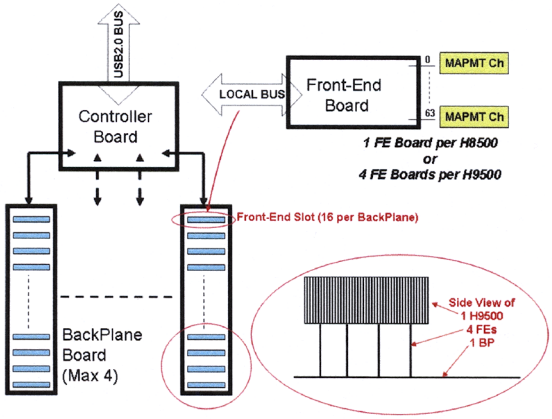


Fig. 1. Schematic of the system structure. On one side, the CB communicates with the DAQ PC by means of a USB 2.0 interface and, on the other side, it can be connected to up to 4 BPs. Up to 16 FEs boards can be connected on a single BP. The FEs are plugged in the proper BP slots and are directly connected to the back side of the MAPMT, as shown in the bottom-right oval of the figure.

The CB can handle up to 4 closely packed Backplanes. Consequently, in its full configuration, the system active area consists of 4×4 H9500, offering a sensitive square surface of about 20 cm × 20 cm with 4096 independent channels. In the SPECT application, the complete system (detectors and electronics) can be enclosed in a 20 cm × 20 cm shielded box.

Array of Hamamatsu H8500 can also be used with minimal changes. In this case the single FE is connected to a PMT device (using an adapter board), and the system can perform the readout of at most 1024 channels.

The electronics communicate with a DAQ PC using a standard USB 2.0 link (Fig. 1). A custom C++ application has been developed to configure and control the system, manage the readout and store event data.

## III. The Front-End Board

The Front-End board is the building block of the electronics, and accommodates the front-end chip, the local FPGA, a delay line and the ADC, as shown in Fig. 3.

The selected front-end device is the MAROC2, a VLSI ASIC, developed by IN2P3-LAL located in Orsay (France) [3]. The chip has 64 independent channels with self-triggering capability and multiplexed output.

Each chip channel has to be directly connected to a MAPMT anode, and is made of (Fig. 2):

- A variable gain preamplifier with low offset and low input impedance.
- A fast shaper with an adjustable threshold discriminator to generate a trigger pulse.
- A slow shaper with a S&H circuit to store the analogue value, proportional to the input charge.

The block diagram of the MAROC2 chip is shown in Fig. 2.

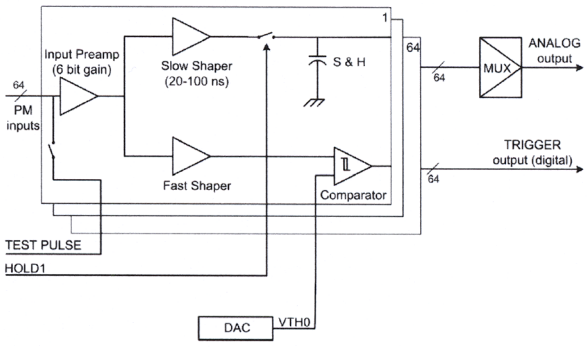


Fig. 2. Block diagram of the MAROC2 chip. Note that the 64 channels have the same architecture, the analog channel values (proportional to channel input charge) are multiplexed on a single pin and the 64 channel discriminator outputs are available to an extern logic.

Each channel has its own digital trigger output. The analogue channel values are extracted individually and serially on a single pin.

The local FPGA, an ALTERA EP2C8F256 device[4], is devoted to handle to the local bus in order to communicate with the CB. It also handles the chip configuration procedure and the readout steps.

During the readout state, the FPGA reads the 64 fast digital signals coming from the chip and runs a trigger discrimination algorithm to enable the acquisition procedure. It can store temporarily in an internal memory both trigger information and channel values. The channel analogue values are digitally converted using the 12 bit ADC chip AD7274 (Fig. 3).

The FPGA generates the *hold* signal to be sent to MAROC2 in order to freeze the charge information in the channel capacitor. The fine tuning of the *hold* signal can be set up by means of a digitally delay controlled line with 1 ns steps.

The FPGA can perform both serial and sparse readout, and can use an external trigger signal to strobe the data acquisition. In sparse readout mode only the values of above-threshold channels are stored. It's also possible to gate the acquisition in order to have an acceptance time window for the triggers (i.e. allowing synchronization with biometrical values).

The FEs exploits a custom synchronous protocol to exchange data and commands with the CB, by means of a shared bus (on a single BackPlane), featuring a 24-bit wide data bus and a 10-bit wide address bus. Moreover an VME-like interrupt[5] procedure has been implemented in order to perform a system event-driven acquisition (each FE can independently informs the CB of an occurred event).

The FE is a very small card: its format (51 mm × 61 mm) matches perfectly with the Hamamatsu H9500/H8500 size.

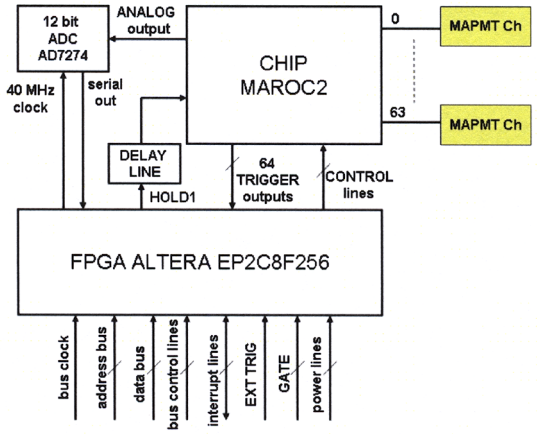


Fig. 3. Schematic of the Front-End Board. The FPGA is devoted to handle the MAROC2 chip, the ADC device and the delay line. It is directly interfaced to local bus lines in order to communicate with the CB.

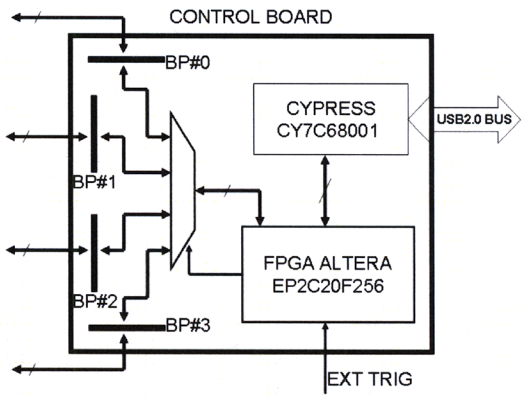


Fig. 4. Block diagram of the Control Board. The FPGA is directly connected to the USB controller in order to exchange data with the DAQ node. Up to 4 BPs can be connected to the CB but the CB can access them one at a time.

## IV. The BackPlane

The Backplane acts as a passive mother board for the FEs and it's directly connected to the CB by means of a short 50 pin flat cable.

The BP feeds analogue and digital power lines to FEs, allows electrical connectivity between FEs and CB by means of the local bus lines, and hosts the active terminations on the signal lines.

The BP can accommodate up to 16 Front-End boards. The FE cards can be directly connected to the back side of the H9500 devices, thus making a continuous sensitive surface of 4 MAPMTs in a row.

## V. The Control Board

The Control Board is the top-level entity in the system.

It exchanges data and commands with each FE board and can manages up to 64 FEs (it is possible to connect up to 4 BPs at the same time). It acts as a single master device on the local bus, so it can address and access to each BP (one at time) and its FE resources.

The block diagram of the Control Board is displayed in Fig. 4.

The main functions are implemented as a firmware running on the local FPGA, the ALTERA EP2C20F256, that is devoted to configure each MAROC2 chip and the related programmable logic, and to manage the readout according to serial or sparse mode.

The CB carries out also the connectivity with the DAQ PC, using a USB 2.0 interface: the FPGA is directly connected to the USB controller (the Cypress CY7C68001, [6]) that manages the USB protocol at physical layer. The firmware reads and processes the 16-bit wide data coming from the USB controller and routes the information to the 24-bit wide local bus, towards the addressed BP/FE. From this point of view, the FPGA acts as an interface between the 2 buses.

The FPGA implements the second level trigger algorithm. During the readout state (both serial and sparse), when a FE card detects an event (successful first level trigger analysis), it informs the CB using the fast interrupt-based sequence. The CB freezes the whole system and starts the readout procedure. The storage of the analogue MAROC2 data is performed locally on each FE card and, at the same time, the CB receives the values of the 64 trigger outputs of the chips involved in the event. The trigger information is used to run a fast second level trigger analysis. If this analysis provides a valid result, the data downloading can start, otherwise, the system is reset. The collected data (trigger outputs state and analogue values) are stored in a file on the dedicated DAQ node.

The described readout approach allows to detect and manage the boundaries effects between contiguous MAPMTs, minimizing the throughput towards the DAQ PC.

## VI. Performances And Test Results

Event processing time is limited by the readout speed of the MAROC2 chip. The time needed for the local data storage in FE FPGA is 32 μsec, regardless of the readout mode. The clock driving the chip output multiplexing is set to 2 MHz. The ADC clock is set up to 40 MHz and the A/D conversion time fits perfectly the chip multiplexing clock.

The local parallel readout of the MAROC2 chips and the 2 level trigger scheme allow to achieve a good acquisition speed: assuming that the average MAMPTs occupancy per event is 5%, the acceptable trigger rate is 25-30 KHz. The USB 2.0 transfer rate fulfils the download speed requirements of the system.

Currently the local bus clock is set to 10 MHz, for debugging purposes. Each FE FPGA uses a simple FAST-OR of 64 MAROC2 trigger outputs in order to implement the first level trigger discrimination, and the second level trigger analysis is bypassed.

The laboratory tests have shown the effectiveness of the proposed approach. Several measurements have been done

using various configurations in order to perform the following detailed functional and noise characterization:

- MAROC2 preamplifier gain and threshold scanning
- MAMPT HV scanning
- Hold delay calibration
- Significant statistic parameters calculation
- Pedestal acquisition
- Single Photon and High Light acquisition using a LED source or a LASER source.

Fig. 5 shows a picture of the system prototype: the Hamamatsu H9500 and related 4 FE boards are well visible.

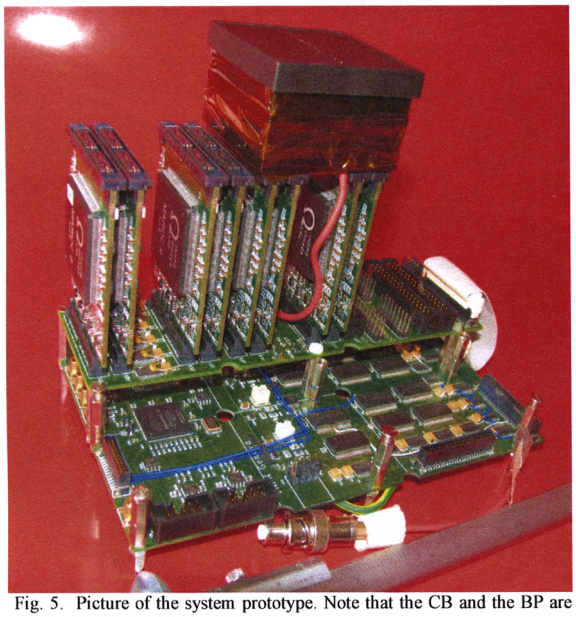

Fig. 5. Picture of the system prototype. Note that the CB and the BP are arranged in order to minimize space occupancy.

An efficient C++ application (using the ROOT framework) has been developed in order to analyse the acquired data. Fig. 6 shows an example of the ADC count distribution of a pixel when the MAMPT is stimulated by a laser source in single photon condition.

As already stated, the electronics can be used in High Energy Physics as imager for RICH detector. The system will be used in 2009 as readout electronics for a prototype focusing Aerogel RICH, developed by INFN Bari and Milano. The first test session will take place in the Test Beam Facility of INFN-LNF in Frascati (Rome, Italy). A system with 2 H9500 devices has been assembled there in October 2008, and some preliminary tests have been performed in order to verify the "in the field" electronics functionalities. Fig. 7 shows the mean ADC count of the 512 pixels when a small LED is used as light source and 2000 events have been acquired. The pixels interested by the light spot are well visible.

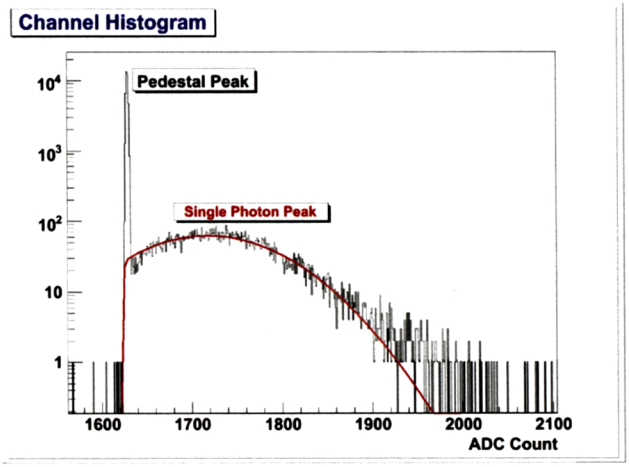


Fig. 6. Example of the ADC count distribution of a channel in single photon condition. The pedestal peak and the single photon peak are well visible.

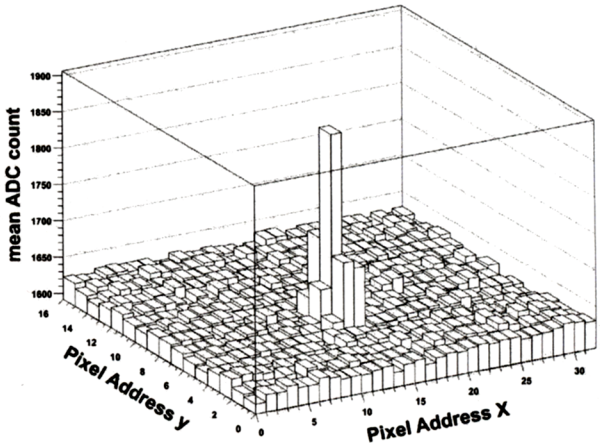


Fig. 7. Mean ADC count of the pixels of 2 H9500 stimulated by a small LED source. The interested pixels are well visible.

## VII. Conclusions

Functional tests have shown good results, but the correlation between triggers and channels values needs further investigation. Further significant tests in laboratory are on the way.

MAROC3 release of the chip, which is pin compatible with MAROC2 but features wider input dynamics and an integrated ADC, is expected in the next months and will be integrated in the system.

The second level trigger analysis has to be implemented in order to improve the event discrimination capability, as preliminary designed

In the near future the bus clock frequency will be set at the design value and a complete SPECT device will be assembled for small animals studies.

The proposed electronics is flexible enough to satisfy, with minor adjustments, the constraints of other applications in the field of nuclear physics experiments and as a readout system for different detectors, such as the very promising Silicon PhotoMultiplier (SiPM), by adapting the FE card to fit the electrical specifications of the detectors.

## REFERENCES


[1] E.Cisbani et al. "Gamma detectors for molecular imaging with radionuclides: design and application", Nuclear Physics B, vol.172, pp. 88-91, 2007

[2] Hamamatsu H-8500 and H-9500 datasheets

[3] "MAROC: Multi-Anode ReadOut Chip for MaPMTs", Barrillon, P. et al, Nuclear Science Symposium Conference Record, 2006. IEEE Volume 2, Issue , Oct. 29 2006-Nov. 1 2006 Page(s):809 – 814

[4] "Cyclone II Device Handbook, Volume 1", February 2007

[5] "The VMEbus Specifications", ANSI/IEEE STD 1014-1987

[6] CY7C68001 EZ-USB SX2 High-Speed USB Interface Device datasheet

[7] ROOT System web page: http://root.cern.ch/root/