Report on LHCb Gain Matching of SPD and PS Multi-anode PMT's

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1 LHCb Calorimeter Design

The SoLID collaboration at Jefferson Lab is considering using multi-anode PMT's (MAPMT) for detection of light from the pre-shower calorimeter. The LHCb collaboration used 64 channel Hamamatsu R7600-M64 MAPMTs for the first two layers of their calorimeter which are the Scintillating Pad Detector (SPD) and Preshower (PS) detectors. These detectors are located in front of the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL) [1]. See Figure 1. The purpose of the entire calorimeter was to provide a first level trigger and (offline) energy measurement for charged particles [2]. This document focuses on the SPD and PS detectors. The SPD is designed to separate charged particles (electrons and hadrons) from photons. The PS identifies electrons and photons. Both detectors are scintillator pads with wavelength shifting fibers. The light is then transported to the MAPMT's using clear fiber. A lead wall of 2.5 r.l. is between the SPD and PS.

The MAPMT's operate with a single HV setting. There is a variation of up to 3x in the gain from channel to channel, but this variation is stable in time [4]. A minimum ionizing particle (MIP) with an average of 25 photoelectrons and pulse length was the particle used for calibration of the SPD and PS detectors.

2 The VFE and FE Electronics

A typical MAPMT pulse shape for a MIP is shown in Figure 2. The SPD and PS detectors have (different) Very Front End (VFE) electronics that are mounted on cards that attach directly to

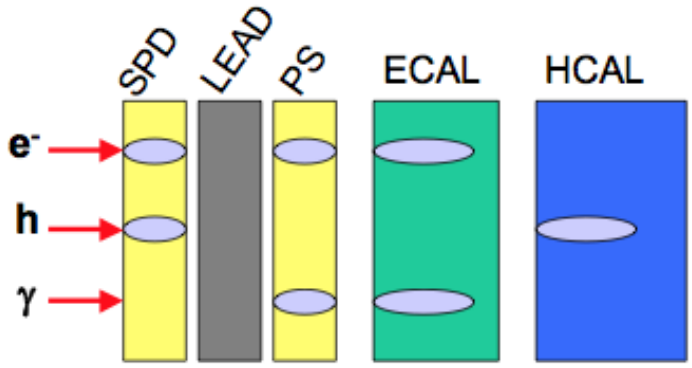

Figure 1: Signal deposited in the different parts of the LHCb calorimeter are shown by the gray ovals.

the MAPMTs. The signals from these cards is sent to a front end (FE) card that is connected by 20-30 m cables. In both cases the first stage of the VFE's amplifies and integrates the signals from the PMT. The integration is alternatively performed by one of two integrators using a 25 ns gate which contains about 85% of an entire pulse. Two integrators per channel are used so that one is measuring the tail of the previous signal while the other is integrating the first 25 ns of the current signal. The 25 ns gate corresponds to the bunch crossing rate of 40 MHz. This two-integrator scheme is used to correct for the part of the tail that lost each time during integration. The integrated signals from the SPD VFE cards are discriminated and a logic pulse is the output which indicates whether or not a charged particle was detected. The integrated signals from the PS VFE cards are sent to the FE cards where they are digitized by ADC's. See Figures 4 and 5

2.1 SPD Calibration

The integrated signal from the SPD is passed to a discriminator which issues a digital yes/no signal indicating whether a charged particle passed through or not. Each individual channel has an adjustable threshold which is set to 0.7 of the MIP peak by a DAC. Because each channel will have a slightly different gain/response, the thresholds are set by performing a threshold scan. First a very low discriminator threshold is set for a given channel and, using a fixed time window, MIPs are counted (for example, N hits are recorded). The discriminator threshold is then raised and the number of hits N' is again recorded. This process is continued for increasing discriminator threshold until the ratio N'/N makes a transition from 1 to 0. The derivative of this data allows one to identify the MIP peaks and set the threshold accordingly [1, 2]. The thresholds are set channel by channel in the VFE cards from a lookup table. The discriminator output was then sent to the FE cards to form a trigger with other necessary signals.

2.2 PS Calibration

For the PS detector, the VFE's integrate the signals and send the analog output of the integration to the front end (FE) electronics where they are digitized by an ADC. These digitized signals were then sent to a Data Processing unit where (digital) corrections were made for each channel to compensate for pedestals and gain variations between each of the channels of a MAPMT. The application of the corrections was described as a slow process and therefore not useful for a trigger. The corrections for each channel were chosen offline so that the MIP signal was at ADC channel 10. These corrections were stored in a lookup table.

3 LED monitoring

Each detector element was equipped with an LED. Because the light output from each LED differed, it was not possible to do an absolute calibration with this system. It was useful however, for setting approximate gain and threshold corrections, and identifying dead channels.

4 Impact on SoLID

From this brief review of the LHCb literature, we understand that to use the MAPMTs for SoLID will require the implementation of custom front end electronics. First, the signals need to be amplified and integrated. This is necessary to deal with variations in the signals themselves and to prolong the life of the MAPMT by lowering the HV. Digital (discriminated) signals can be corrected for variations in the response/gain of individual detector elements by having independently adjustable discriminator thresholds for each channel. This can be done at relatively high rate for use in a trigger. Proper thresholds must be determined using threshold (rate) scans. The analog integrated signals from the MAPMTs are sent to an ADC followed by a processing system which applied corrections to the digitized signals to correct for gain variations and pedestal offsets. The VFE and FE cards are necessarily complex and require both analog and digital signal processing, along with addressable custom modules for setting thresholds, pedestal and gain corrections and also for setting timing. Implementation of MAPMTs for SoLID will require substantial investment in front end electronics development.

References

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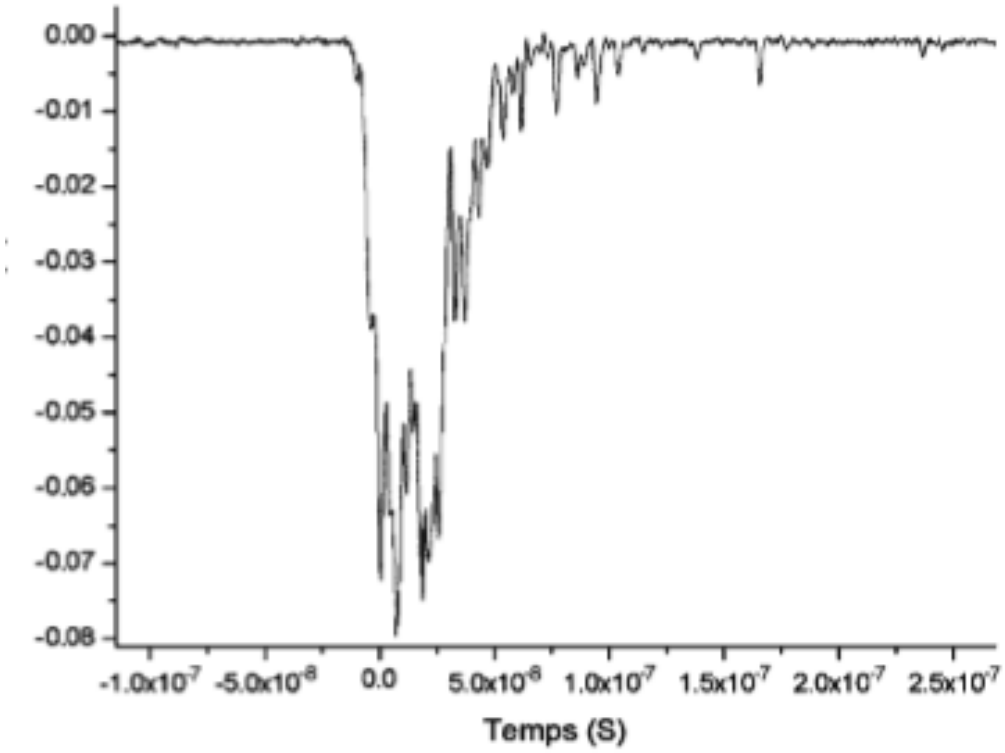

Figure 2: Typical raw MIP signal from a MAPMT channel.

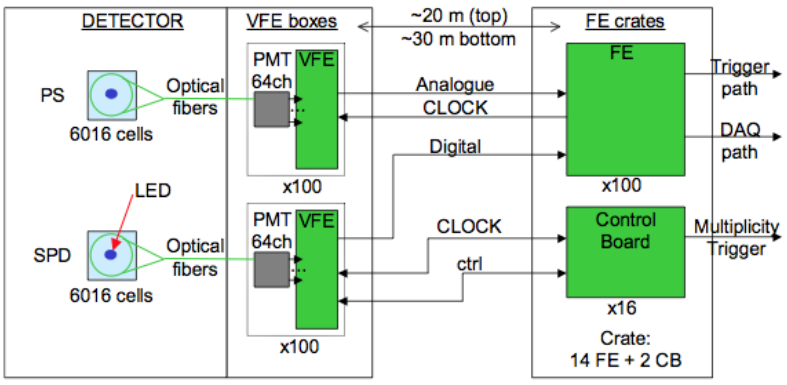

Figure 3: SPD/PS electronics readout scheme.

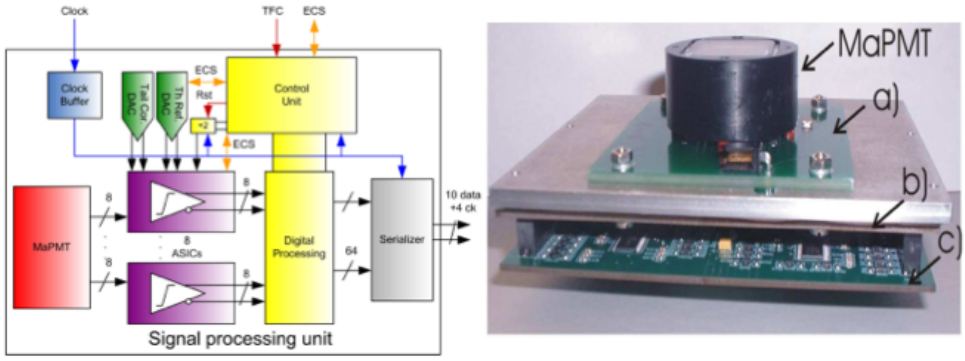

Figure 4: Left: Block diagram of the SPD VFE card. Right: MAPMT mounted to card a), followed by ASIC card b) followed by FPGA control card c).

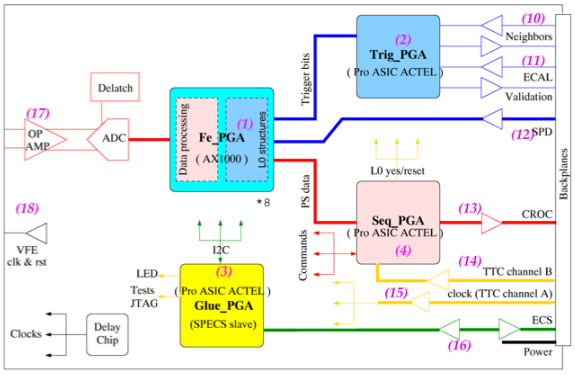

Figure 5: Block diagram of the front end (FE) electronics where the PS signals are digitized by and ADC and the subsequently corrected for gain and pedestal variations channel by channel (Data Processing).