8 Electronics and readout

8.1 Introduction

In current design the Cherenkov radiation is collected on a large array of MAPMT H8500; the total number of independent channels per sector is expected to be 25600, thus requiring highly integrated front-end electronics with modular design. In fact the impact of the electronics material on the detectors downstream the RICH must be minimized, in terms of background and particle straggling at least.

A typical modern architecture of the readout electronics consists of front-end cards with dedicated Application Specific Integrated Circuit (ASIC) configured, controlled and readout by programmable devices such as Field Programmable Gate Array (FPGA) either close to the front-end or onto the acquisition node depending on the ASIC features and the specific needs in term of real-time processing. The choice of the ASIC candidates has to be driven by the fulfillment of the detector requirements, the availability of on-the-shelf components or availability after minor development (no brand new development) and the existing experience within the collaboration.

Performance and status of different chips have been analyzed. Promising and interesting new developments such as VMM1 chip at Fermilab [24] and CLARO chip at INFN Milano [25] have been dropped due to the early development stage. Other more consolidate potential candidates such as the higly compact APV25 [26] have been excluded since cannot satisfy all requirements. The 64 channel DREAM [27] chip, working in analog sampling mode, could be a potentially interesting solution, even though it necessitates some additional developments for the RICH application. More details will be given in Sect. 8.6. At the end, our final choice is based on the 64 channel MAROC [28] (MAROC is an acronym for Multi Anode Read Out Chip), an ASIC manufactured by Omega Group of LAL (Paris, France), currently at version 3 (MAROC3). This solution satisfies all the relevant requirements and therefore it represents our mainstream option, taking also into account our consolidated experience on MAROC electronics design and operation.

In the proposed design we end up with stacked PCB layers behind each MAPMT sensor. The first layer houses the ASIC front end and ancillary components (e.g. external amplifier) and it is directly connected to the anodes array[3]. A second PCB will host the FPGA in charge of configuring, managing and acquiring one or more ASICs and the low voltage and HV bias distribution. The design foresees the use of the JLab SSP [30] as controller and collector of the front-end data, so that part of the development will have strong synergies with the current JLab upgrade activity. Data are transmitted on high speed serial (optical) lines minimizing the wiring and therefore the material budget.

With that *sandwich* architecture the total photon detection surface will be covered by a fixed number of basic units or tiles made up by two or three sensor each. The total spacing for electronics will not exceed 20 cm in depth (including MAPMT and mechanical support).

In the present analysis, the most relevant issues have been considered, ending up to a conceptual design of the electronics readout. Optimization of all the technical details is in progress.

[3]Decoupling or attenuation lines between anodes and ASIC inputs are considered part of the front end.

8.2 Requirements

Here are summarized the component main requirements that must be fulfilled by the readout electronics.

- **Trigger rate and dead time -** The expected readout trigger rate is 20 kEvents/s; the electronics shall sustain such rate with a dead time smaller than few %.
- **CLAS12 trigger latency -** The maximum CLAS12 trigger latency is 8 μs. The electronics must satisfy this latency and keep track of events that occurred up to 8 μs before the arrival of the trigger in the electronics.
- **SPE sensitivity -** The front end must be sensitive to single photoelectron (SPE). This translates to a minimum detectable charge at the level of few 10^6 electrons (see section 7.1).
- **Number of channels -** One RICH sector will have 25600 independent anodes. The electronics must provide the same amount of readout channels.
- **Anode gain spread compensation -** The electronics shall be able or permit to compensate the gain dispersion among the anodes of the MAPMT that typically is around $1:2$ but that can be as high as $1:4$ (see section 7.3).
- **Crosstalk -** Crosstalk between electronics channel should be smaller than the photodetector crosstalk (see section 7.2). A level of 1% is considered acceptable.

The front-end electronics, mounted behind the photon detector, shall cover the photon-detector area at maximum and shall have a total thickness not larger that 10 cm. This relatively small space may impact on heat dissipation and therefore the electonics must have a power consumption as small as possible. Being invested by the same dose rate of the rest of the detector (see section 12.2), the ASIC and all active components (voltage regulators, transceiver, FPGA) must be radiation-hard.

The temporal development of the MAPMT signal allows a time resolution below 1 ns (Transit Time Spread for H8500 is around 0.4 ns [32]). The dark noise rate goes up to 1 kHz per MAPMT with typical level below 500 Hz (see section 7.4), and therefore its contribution to the background rate is negligible for acquisition window at the level of few hundred ns (hit/event on the whole sector $\ll 1$). The main restriction on the time resolution comes from the possibility to disentangle the direct and reflected photons whose time difference (2 m or more difference in traveling distance) is about 6 ns or slightly more. Therefore a time resolution of the order of 1 ns would be very appreciated to help the reconstruction program but is not a stringent requirement.

8.3 MAROC Front End electronics

The MAROC [28], has been originally designed for the ATLAS Luminometer in AMS 0.35 μm CMOS technology and is currently in a well consolidated, production phase. The block diagram of the MAROC internals is reported in Fig. 40 while the main specifications are in Tab. 4.

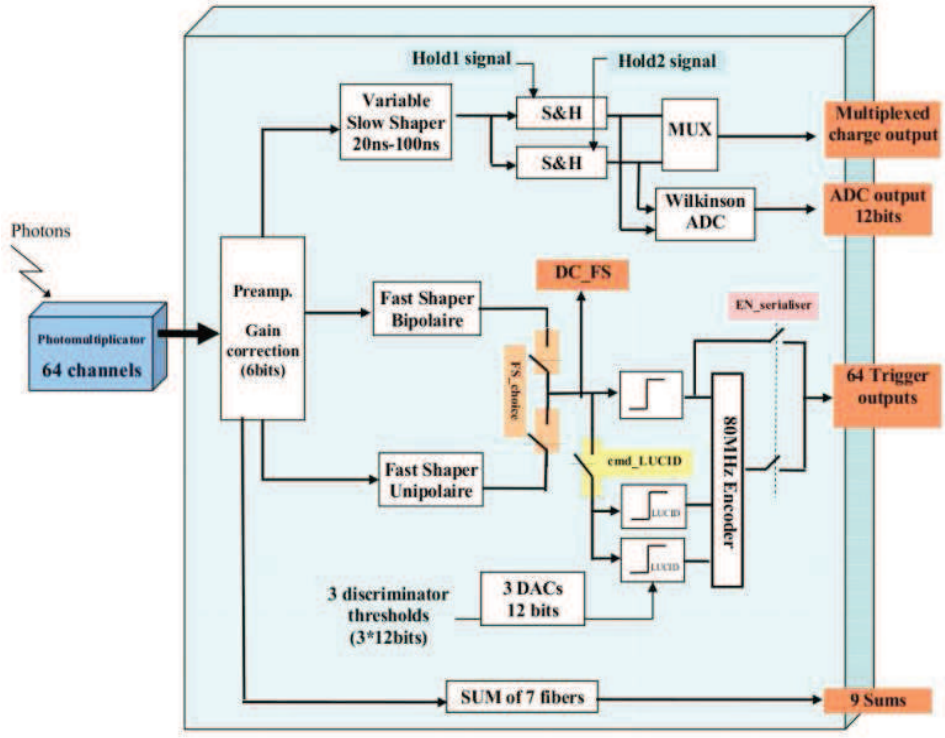

Figure 40: MAROC block diagram.

The chip consists of 64 independent channels and provides both the analog and binary (digital) information of each channel. The single channel has a pre-amplification and configurable 8 bit gain correction stage followed by three independent lines:

- a binary line with a fast shaper ($\sim$ 20 ns peaking time) followed by a discriminator with configurable threshold designed to provide 100% efficiency at one third of photoelectron;
- an analog line with a slow shaper ($\sim 30-210$ ns) followed by two track and hold circuits that permit the charge measurement through a serial multiplexing (single analog output of the 64 channels);
- a third line converges on one of the 8 embedded analog sums; each sum collects up to 8 consecutive (and selectable) channels. [4]

[4]The sum signals are expected to have a time resolution similar to the PMT's intrinsic resolution.

Table 4: MAROC3 and DREAM specifications.

Spec	Unit	MAROC3	DREAM
Technology		AMS 0.35 CMOS μm	
Number of channels	ch	64	64
Input polarity		neg.	pos. and neg.
Max Input dynamics	fC	5000 (30 p.e.)	50 - 1000 (4 steps)
Variable preamp. gain	bit	8 (0-4)	2
Analog output		MuX (5 MHz)	MuX Diff. (20 MHz)
Analog Shaping Time	ns	20-100	50 - 1000 (16 steps)
Analog Pipeline Size	cell	1	512
Pipeline Frequency	MHz	none	1 - 50
Binary output		64 parallel	OR only
Digital Shaping Time	ns	10-20	50 - 1000
Threshold range	bit	10	8
100% Trigger efficiency	p.e.	1/3 (50 fC)	-
Noise	fC	2	-
Linearirty	%	2	< 2
Cross talk	%	1	-
Power consumption	mW/ch	3.5	10

The binary information of the 64 channels are available as parallel outputs that can be synchronized with an external trigger (EXT mode) or used as self generated trigger (SE mode). Both fast and slow shapers are highly configurable in terms of peaking time and dynamic range.

The MAROC needs 20 I/O lines for its configuration and readout (+ 64 independent lines for the binary information), including both the charge output fed into an external ADC and the internal Wilkinson ADC output. Some of the 18 lines (HOLD signals, ADC RESET, ADC Clock, and 3 additional levels) can be paralleled on more chips, while other can be daisy chained (Multiplexed output control, SLOW Control). Therefore, of the 20 I/O channels, 5 lines need to be connected to each single MAROC independently (+ the 64 binary hit bits), while the others can be shared by multiple MAROCs.

Charge measurement The charge measurement through the analog line requires an external "HOLD" signal within about 200 ns (maximum HOLD latency) from the event, which will freeze the charge on an holding capacitor that can be subsequently readout in a serial multiplexed way (with up to 5 MHz clock) either as an analog value or converted to a digital value by an internal Wilkinson ADC. The relatively small HOLD latency makes impossible during normal acquisition the use of the MAROC analog lines in the CLAS12 RICH. The analog information can be used for calibration purposes, in dedicated runs or in a restricted way during normal acquisition.

Binary information On the other hand the digital line is suitable for the RICH application; the binary information of each channel is promptly available in parallel and can be sampled with a predefined clock on a adequate deep external digital pipeline. The sensitivity of the threshold, its stability and the noise of the digital line have been measured; results are presented in section 8.4.

The digital information of each MAROC consist of 64 bits/events or 8 bytes/event which corresponds to 3200 bytes/events of the whole single sector; this size combined to the 20 kHz event rate can be easily managed by any modern DAQ such as the SSP based. Even in a simplified architecture where all MAROC data words are fully serialized, the total data rate is at the level of 64 Mbytes/s which are easily sustained by many modern serial link.

A precise time measurements can be obtained from the 8 MAROC sum lines fed into a fast amplifier (e.g. NINO [33]) followed by sub-nanosecond TDCs.

For its initial application in ATLAS the MAROC has been designed to be radiation tolerant, using the suitable AMS 0.35 μm CMOS technology[34], and therefore we expect no radiation issues. In any case we intend to test the radiation tolerant capability of the final electronics in a neutron radiation facility.

8.4 MAROC test and characterization

All MAROC tests have been conducted on the existing implementation designed by members of our group for applications in nuclear medicine[35]. Such implementation is optimized for many optical photons detection in self generated trigger mode, and analog readout. However it already includes several features suitable for the CLAS12 RICH: compactness, modularity (front end with ASIC and FPGA linked to a separated controller board), low power consumption, easy coupling with Hamamatsu H8500. Single photoelectron capabilities have been investigated by many tests in laboratory using laser source at single photoelectron level and under charged beams in different readout modes.

The read out system has been successfully used in analog mode and in external trigger in the RICH prototype test at CERN in 2012 (see Sect. 11). After that, an upgrade of the FE cards has been performed and in July 2013 a dedicated test has been conducted at the Frascati BTF to mainly characterize the binary readout in experimental conditions with Cherenkov light.

As shown in the following sections, all those tests and characterization confirmed the excellent single photon capabilities both in analog and binary mode, making it a suitable candidate for the RICH readout.

8.4.1 External mode: Analog response

Figure 41 shows the analog response of a single pixel illuminated by a laser pulse (emitted at $t \sim -20$ ns) at single photoelectron level for different delays of the sampling relative to the trigger. The shaped pulse is bipolar as expected showing two local maxima (in absolute value): the first is positive and ensures the largest precision to the charge measurement but it occurs pretty early (20-30 ns); the second, with opposed polarity, has less dynamic range

but it offers additional 100 ns to the trigger latency[5].

Actually the earlier maximum cannot be used in typical experimental conditions where the trigger formation takes longer than ~ 50 ns from the occurrence of the physical event, as in the CERN prototype test setup where the acquisition was synchronized with the second maximum. The good results presented in Sect. 11 demonstrate the adequacy of the chosen conditions, although they are not optimal.

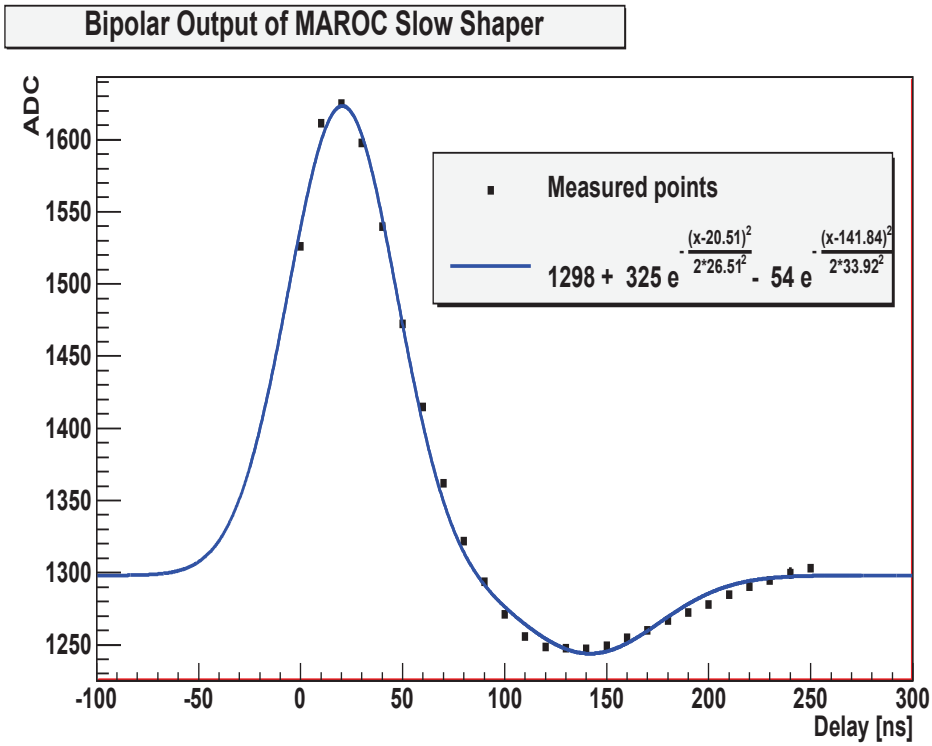

Figure 41: Slow Shaper output waveform reconstructed

8.4.2 External mode: Binary signal

MAROC binary information comes from the discrimination of the output of the fast shaper lines. The characterization of the quality of such information (in terms of single photo-electron detection capability) has been conducted correlating the binary and analog data, varying (and optimizing) essentially the discriminator threshold (common to the 64 MAROC channels), the synchronization time between the analog and binary lines and the pre-amp gain, both in self (calibration) and external (experimental) trigger modes, with and without laser source.

Figure 42 shows the SPE spectra (with pedestal) of a single MAROC channel, illuminated by a laser source at SPE level taken on the first analog maximum. This represents the optimal

[5]In case of saturation the second maximum could shift in time compromising the synchronization with the trigger.

conditions which are possible by the availability of a pulse that trigger the laser source. In red the events recorded on the analog line, which are at the same time above threshold in the binary line (those that provide the binary "1" response).

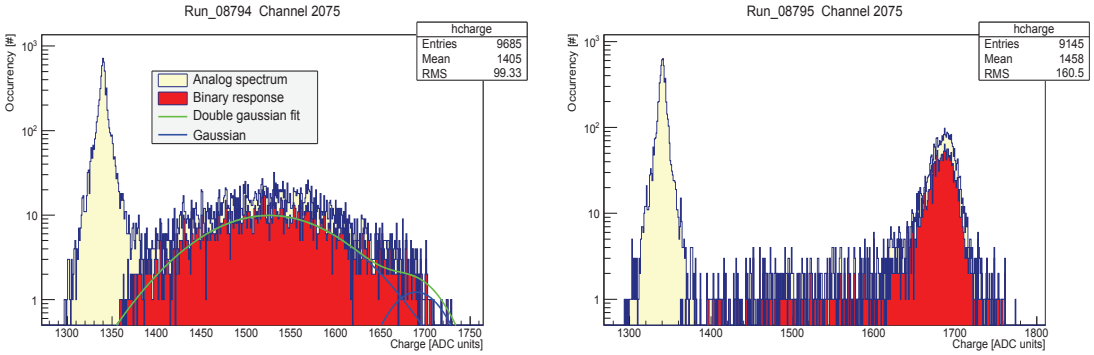

Figure 42: SPE spectra at different gain, over threshold events in red. Left plot unit gain, right plot gain = 4

The separation between signal and pedestal is very clear already with gain $G = 1$ (left plot), as highlighted by the red binary events demonstrating the excellent sensitivity of the binary readout to single photon. At gain $G = 4$ (right plot) the analog is getting saturated but the binary data are still remarkably good. The small mismatch between the two histograms (binary inefficiency relative to analog) in the overlapping region (above pedestal) is due to a non optimal relative synchronization between analog and binary readout, as will be discussed at the end of this section.

Figure 43 reports SPE spectra on the second maximum. Here, the SPE region appears on the left side of the pedestal due to the shaping of the input signals. In red we show the binary signal at three different thresholds. In this case binary and analog lines are properly synchronized. Although the separation of the analog line is slightly worse than in figure 42, as expected (due to the selection of the second maximum) the binary cut is still of impressive quality (middle plot).

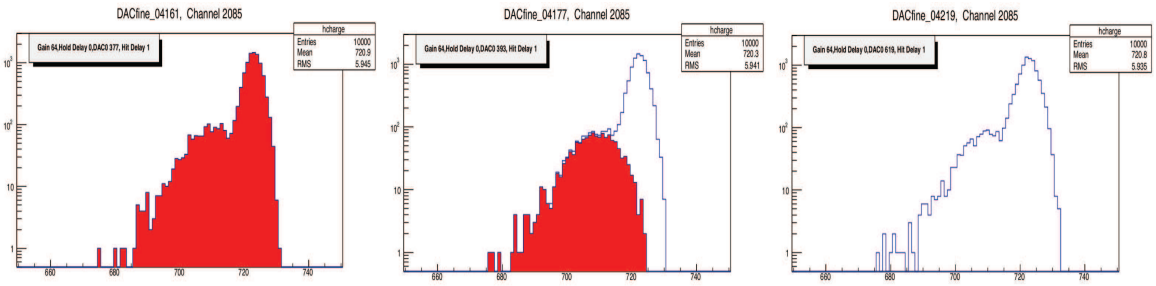

Figure 43: MAROC charge spectrum at single photoelectron level in external trigger mode using three very different digital thresholds (DAC values); threshold increases from left to right. The red histogram represents events with binary signal.

Figure 44 shows the effect of the analog-binary synchronization time on the SPE spectra; when the synch is not optimal the red histogram (binary signal) does not completely overlap the full spectrum above the pedestal because analog and binary are looking at slightly different times. Current MAROC electronics allow a 25 ns step for tuning.

It is worth to point out that in the final operating conditions (binary readout) the analog information will be basically used only for calibration purpose in self trigger mode where the analog-binary synchronization is not an issue or as estimation of the common noise, which does not require synch between the two lines.

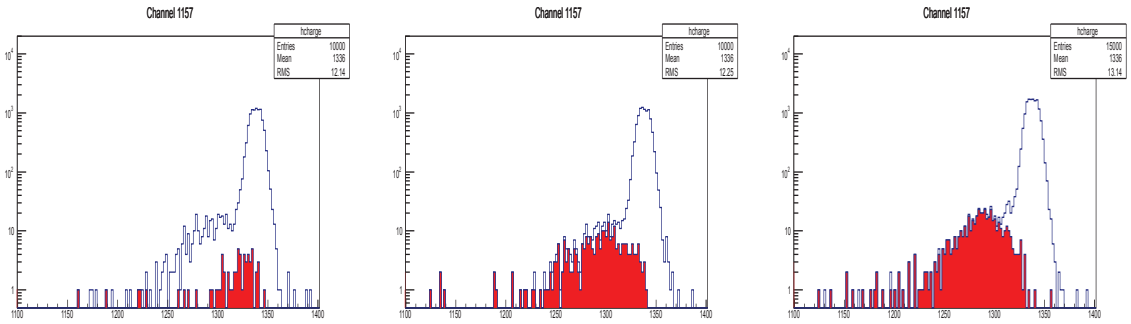

Figure 44: SPE spectra at three different synchronization time (25 ns step) between analog and binary lines.

8.4.3 Dark count and SPE in self trigger mode

The binary readout combined to the self trigger capability offers the possibility to measure rather quickly the dark count of the individual MAPMT channels, get information for the equalization of the channel gain and define the optimal threshold. Figure 45 reports the acquisition rate (not corrected for CPU busy time) versus the binary threshold level in case of laser source off and on, acquired in self trigger mode, only one MAROC channel enabled. The noise region is clearly evident in both source conditions. Dark count rate of the single anode is at the level of $10 \div 20$ Hz as expected from MAPMT specification and it extends roughly as the SPE signal with laser light on. The SPE region is pretty large, showing that the threshold level is not very critical, and count rate decreases rather slowly indicating that the fast shaper is probably working in a sort of saturated regime.

It is worth mention that the measurement of the dark rate spectrum as a function of the binary threshold can be adopted for the calibration of the combined system MAPMT plus electronics. In fact the drop of the noise region can be easily detected and all channels can be equalized (via the gain setting) to the noise drop at the same (or nearly) threshold value thr_n. Once this is done the optimal threshold is chosen as $thr_s = thr_n + k\sigma_{thr}$ where k is a reasonable factor (2 or 3) and σ_{thr} is the width of the noise drop (estimated either on the count rate derivative or the distance between 10% and 90% of the drop).

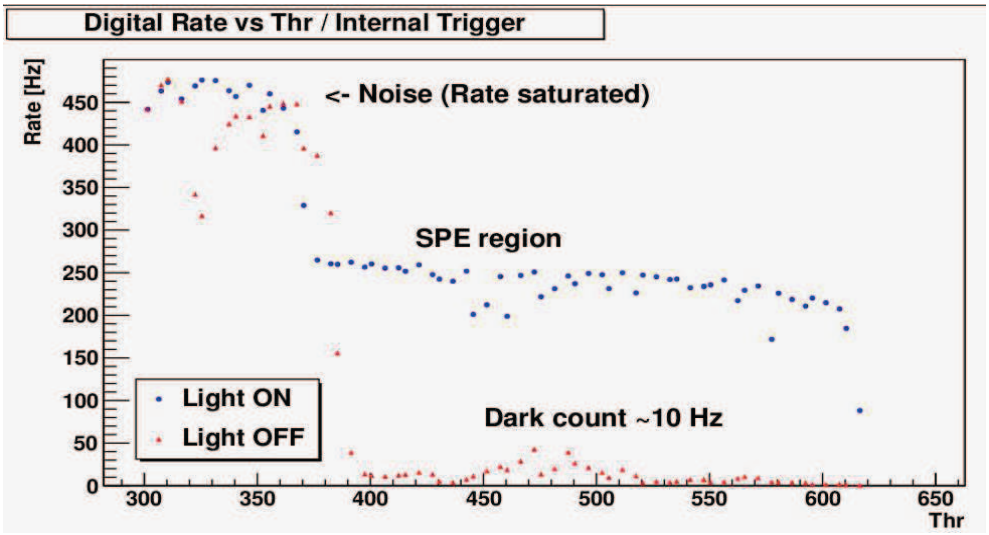

Figure 45: Acquisition rate in self trigger mode with laser trigger on and off.

8.4.4 Gain equalization by thermal noise

The use of the self trigger capability of the MAROC can be further exploited for calibration purpose, measuring the thermal (dark) spectra of each anode. Figure 46 shows dark spectra of two different channels acquired in self trigger mode with timing tuned on the first maximum of the analog pulse. Considering the small dark count rate, a similar measurement in external trigger would require much more time, unless one uses an external light source as in figure 42. This kind of spectra can be analyzed by an automatic procedure to equalize the gain of each channel and again to select the proper discrimination threshold. It represents a tuning gain and threshold procedure in addition to the one discussed in the previous section.

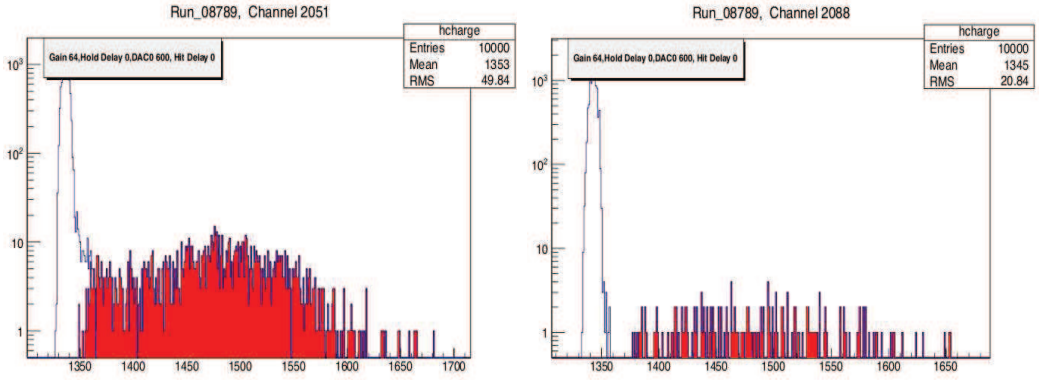

Figure 46: Dark spectra for two different channels. Analog timing calibrated on the first (positive) maximum of the analog waveform.

8.4.5 Effect of cabling on noise level

All RICH prototype tests have been performed connecting the MAPMT to the electronics front-end by flat, high density, shielded SAMTEC cable, 1.5 m long (HQCD series), see for example Fig. 47. This configuration is imposed by the layout of the existing MAROC electronics and the MAPMT on the RICH prototype. In the final RICH, electronics will be directly connected to the MAPMT, avoiding a potential source of relevant noise. In fact figure 47 shows the measured noise level (RMS of pedestal of the analog data) in the laboratory for different cable length and electronics gain. It is clear that without cable the noise is basically absent independently from the experimental conditions. Most of the noise is related to a common effect and can be largely suppressed by offline analysis of the analog data, averaging a consistent number of channels and subtracting to each channel value the mean value. This procedure has been applied in the analysis of the CERN test beam data, however it must be taken in mind that it may reduce the dynamic range of the data and that it cannon be applied to the binary data.

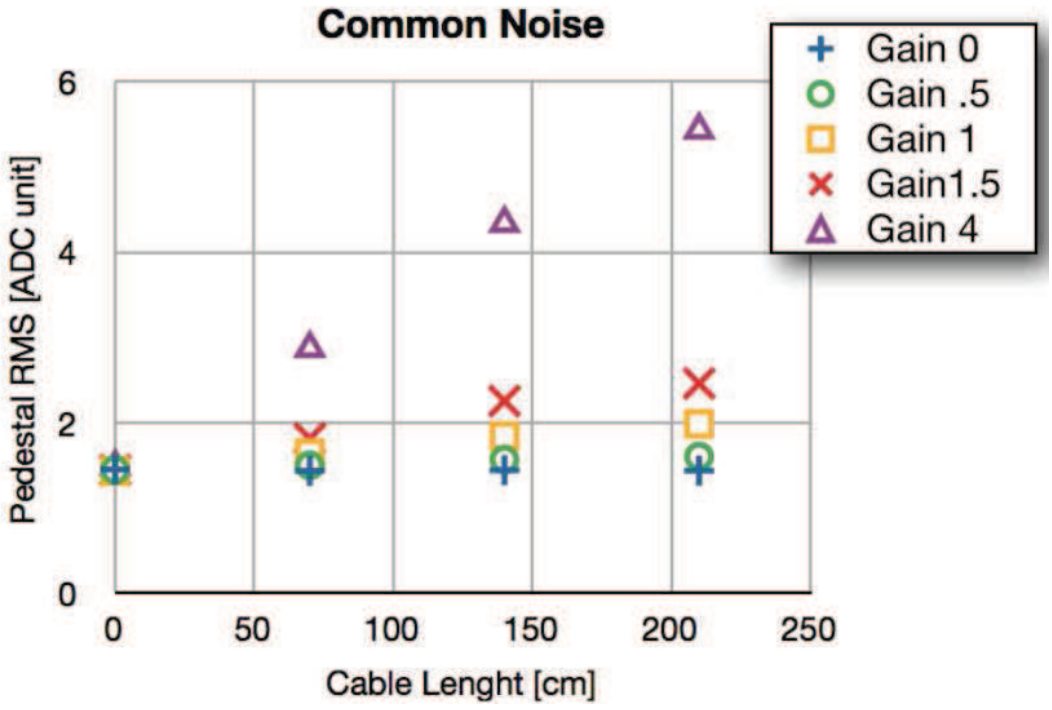

Figure 47: Noise effects of the cable length connecting MAPMT to the front-end electronics. Note that this noise level is significantly dependent on the experimental condition.

8.4.6 Power consumption and heat

MAROC power consumption is small as 3.5 mW/ch and the current INFN electronics consume a bit less than 0.5W, so for 400 of them we estimate a total absorption of 200W. Including all the components, the total power consumption won't exceed 400W.

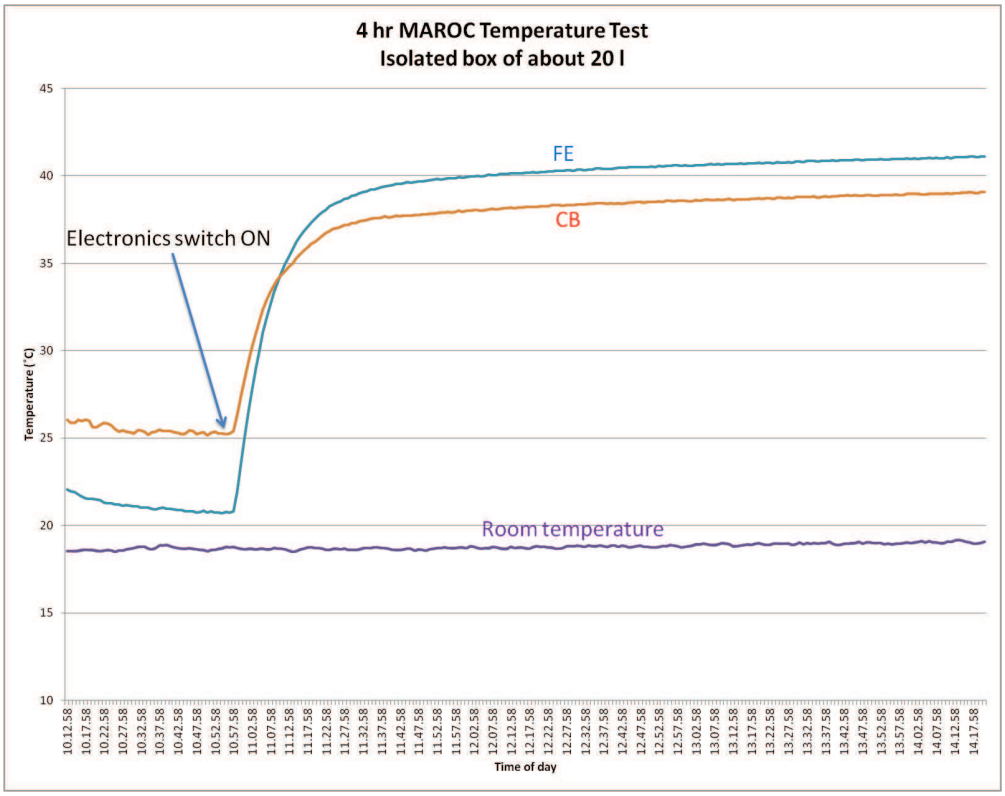

Figure 48: Results of a 4 hours test of the MAROC Electronics regarding heat production and dissipation. Eight Front End (FE) cards have been mounted on two Control Boards (CB). The set up was closed inside a sealed container of about 20 l volume, without any cooling, held inside a room at constant temperature of 18 Celsius.

A first thermal test of heat production and dissipation of a MAROC set up having 8 Front End (FE) cards on two Controller Boards (CB) has been done in July 2013 using a sealed container with a volume of 20 liters, without any cooling, putted inside a constant temperature room held a 18 Celsius. The result was that the temperature close to the FE reached an equilibrium temperature never exceeding 42 Celsius for the FE and 39 Celsius for the CB (see Fig. 48). Note that when the electronics was switched ON the air inside the container was above the room temperature. The temperature probes were directly put in contact to one of the FE cards and in an interstice of the CB in order to measure the temperature in the worst situation. Further test are foreseen in the next months.

If needed, dissipation of this heat will be performed in the RICH by flowing fresh air inside the electronics housing.

8.5 DAQ Electronics: from PMTs to DAQ modules

In the present preliminary design, the DAQ electronics is composed by three logical (and actually physical) layers; the block diagram of the first two layers and connection is shown in figure 49.

1. ASIC Board: it hosts the front end MAROCs, 8 channels fast amplifiers (such as the NINO chip[33]) for the MAROC sum lines, a DAC for the discriminators of the amplified sum lines, the MAROC bias circuitry, a common delay line (for the HOLD signal) and the connectors toward the PMT and the upper layer. One card will serve up to three PMTs. The card is directly connected to the PMTs to minimize possible source of noise as discussed in section 8.4.5. In this scheme, the analog response of the MAROC is used only for calibration and assumed to be converted to digital information by the internal Wilkinson ADC. The ASIC Board needs to connect up to 284 lines with the FPGA level as detailed in table 5; however, the OR lines can be suppressed without any relevant impact, as well as the external ADC. The differential NINO output can be converted to unipolar (LVDS-LVTTL) with marginal temporal degradation; in this optimized scheme, the total lines to be connected are 245.

2. FPGA Board: it hosts a capable FPGA (e.g. Xilinx Artix-7 XC7A100T with 285 I/O and 4 Gigabit Transceivers) which will configure the front-end MAROC, distribute the trigger, read the front-end, provide the proper input registers (64 for each MAROC) with adequate (8μs latency) pipeline and TDC functionality (with resolution of at least 1 ns). In addition an electrical-optical transceiver will permit the transmission over a fast optical line toward the DAQ board of the next layer. A single FPGA Board will manage up to 3 MAROCs, thus reducing the optical link and exploiting effectively the FPGA resources. The FPGA Board will also contains the distribution lines of the HV (to the PMTs) and Power (+5 VDC and Ground) to the ASIC Board.

3. DAQ Board: it consists of the standard CLAS12 SSP VXS module in charge of controlling and acquiring data from up to 32 FPGA boards by fast optical links. The FPGA boards will be compliant with the SSP specifications and transfer protocol.

With this scheme in mind, assuming that:

- each binary channel transition has a 13 bits time information associated (with 1 ns resolution, 13 bits provide 8192 ns time range)
- each MAROC sum line has a 14 bits time information (0.5 ns resolution),
- the maximum hit occupancy is 20% (safe value),
- a fast 2.5 Gbps serial link,
- the multiplexing MAROC factor of 3 (up to 3 MAROCs on one optical link),

the expected readout time (from MAROC to SSP transmission time) is:

$$(13\,bits \times 64\,channels + 14\,bits \times 8\,sums) \times 0.2\,occupancy \times 3\,\frac{MAROCs}{board} \times \frac{1}{2.5GHz} \sim 230ns \tag{10}$$

that corresponds to a dead time of $\sim 0.5\%$ at 20 kHz.

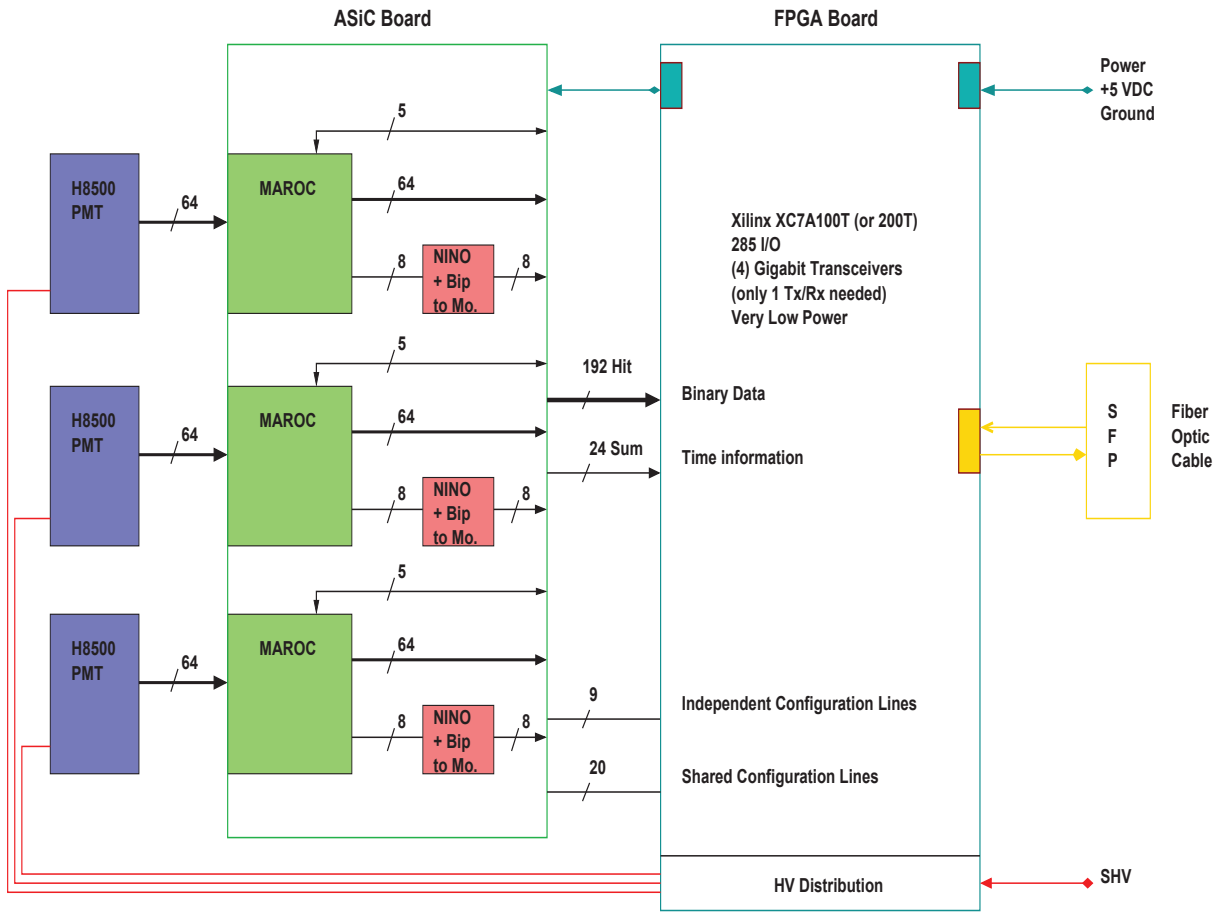

Figure 49: Readout Electronics Block Diagram; optimized connection between ASIC and FPGA Boards.

8.6 Alternative option: DREAM

The excellent MAROC performances measured in the above-reported tests and characterizations (as well as in the RICH prototype test at CERN) are more than satisfactory for the operation of this chip in the CLAS12 RICH and therefore MAROC represents the current mainstream choice as front-end chip in the RICH readout electronics.

However, potential costs and resources optimization can still be obtained adopting the alternative 64 channel DREAM ASIC[27] under development for the CLAS12 Micromegas and therefore well fit into the CLAS12 DAQ without significant additional effort from the RICH collaboration. The chip architecture derives, in part, from previous developments made for the AFTER and AGET chips[31].

The block diagram is shown in fig. 50 and specifications are in table 4.

The DREAM collects, amplifies, filters, discriminates and stores the analog signal of the sensor in an analogue 512 deep memory. The sampled signals, marked by the trigger, are read-out asynchronously without affecting the analogue memory storage; in this way the pipeline guarantee a deadtime-free operation for trigger rates up to 20 kHz. The sampled

Group	I/O lines	Purpose	Connection	Comment
Signal	64×3	MAROC/HitBit	independent	
	16×3	NINO/Output differ.	independent	if unipolar 8×3
	2×3	MAROC/OR	independent	unessential
	2×3	NINO/OR differ.	independent	unessential
Config	3×3	MAROC/ADC Control	independent	
	4	MAROC/Slow Control	daisy chain	
	4	MAROC/MUX Out	daisy chain	
	2	MAROC/HOLD	parallel	
	3	MAROC/ADC RST, CLK	parallel	
	1	MAROC/EN_OTAQ,	parallel	
	1	MAROC/CTEST	parallel	
	1	MAROC/VDD_FSB	parallel	
	2	DAC/I2C	serial/shared	
	3	Ext. ADC/SPI	serial/shared	optional
	2	Delay/Conf	shared	
Total(A)	284	no optimization		
Total(B)	269	no OR, no ext ADC		
Total(C)	245	no OR, no ext ADC, unipolar NINO output		

Table 5: ASIC Board pinout

signals must be digitized by an external ADC.

The main differences between the MAROC3 and DREAM chips are:

- input dynamic range in DREAM is optimized for gaseous detectors and therefore typically smaller than for a PMT output;
- DREAM hosts a long (512 cell) analog pipeline for each channel with sampling clock up to 50 MHz; this permits to have a trigger latency up to $\sim 10\mu$s;
- DREAM gain can be adjusted in 4 steps only (instead of 8 bits excursion in MAROC); the analog output allows monitoring and correcting for the anode dis-uniformity;
- the DREAM binary output is the sum (OR) of the 64 discriminated analog levels (while MAROC offers all 64 channels);
- DREAM analog data can be readout at 20 MHz, allowing to sustain a trigger rate up to 20 kHz (with 4 samples/trigger);
- the ADC that converts the analog DREAM levels must be provided by the readout electronics (MAROC has an internal, rather slow ADC converter).
- the DREAM project is in a consolidated development phase, while MAROC is already at the 3rd version.

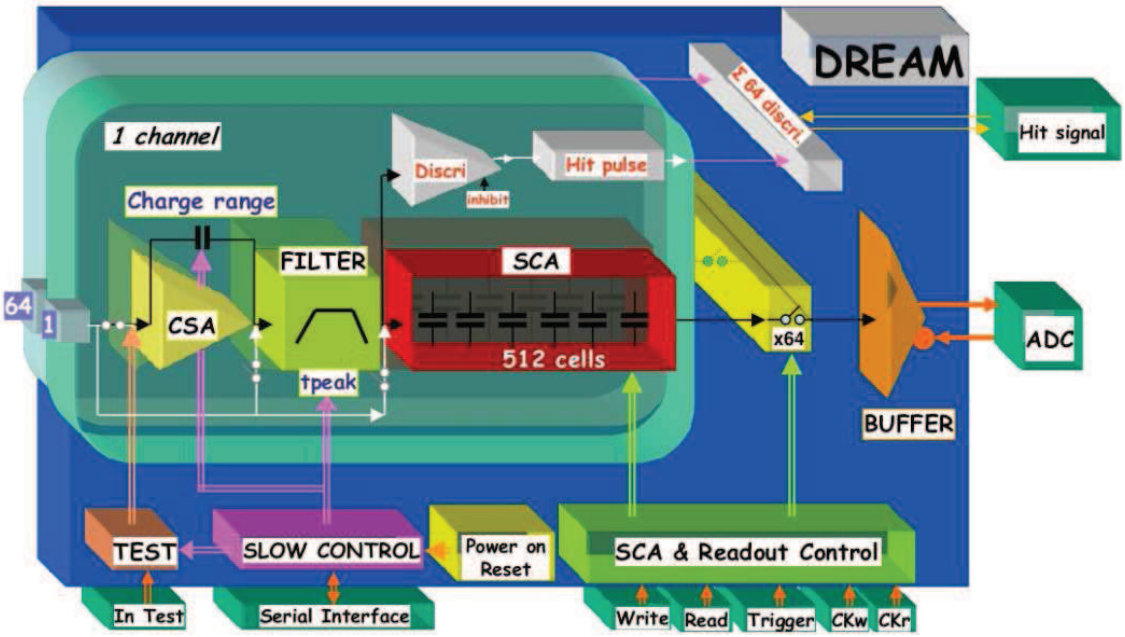

Figure 50: DREAM block diagram.

The DREAM offers a modest time resolution which can be evaluated to about 6 ns (the minimum shaping time divided by $\sqrt{12}$). Similarly to the MAROC chip, the sum of the binary signals can provide an improved time resolution, which must be measured.

In order to match the PMT output to the DREAM input the passive adapter board shown in fig. 51-left has been designed and realized. The board will attenuate the PMT signal (if needed) and reduce the parasitic coupling between the channels. A schematic diagram is shown in Fig. 51-right.

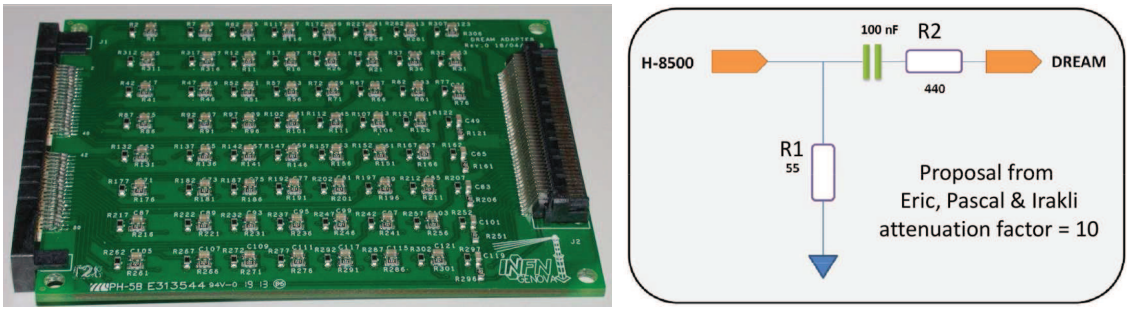

Figure 51: MAPMT-DREAM adapter board.

Test of the DREAM option are planned by the end of the year.