CLAS12 RICH Frontend Electronics

Outlook

- Requirements
- Description of MAROC ASIC
- MAROC Tests and Results
- Front-End Electronics for RICH
- Conclusions

M.Turisini (JLab)
P. Musico (INFN-Genova)
E. Cisbani* (INFN-Roma/ISS)

* Speaker

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Jefferson Lab

INFN

Requirements (for PMT readout)

Single photoelectron sensitivity	~50fC
Number of channels per sector	25600
Anodes gain spread compensation	1:4
Event Rate	20 kHz
Dead Time	few%
CLAS12 trigger latency	8 μs

Time resolution ~1 ns

To disentangle direct and reflected photons (can be done off line)

Compactness/ Power consumption

Max area 1 m^2, max thickness 10 cm, power consumption compatible with air flow heat dissipation

Radiation hardness

Must operate in the same irradiation level of the MAPMTs

ASIC choice

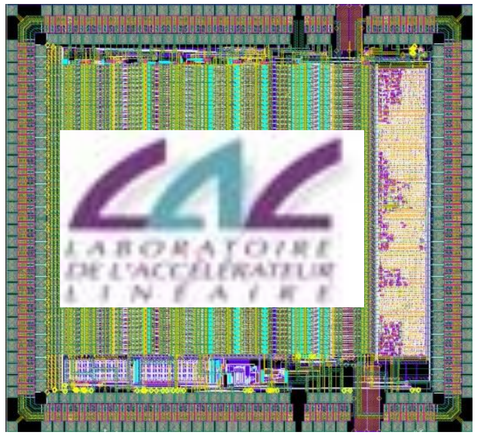
- On-the-shelf components (no brand new development)
- Fulfill the requirements
- Existing expertise in the collaboration

✗	VMM1/FermiLab	not consolidated , interesting specs
✗	CLARO/INFN	early stage, few channels
✗	APV25/CMS	not enough latency
✓	DREAM/JLAB	CLAS12 Micromegas
✓	MAROC3/LAL	ATLAS Luminometer

MAROC3 initially used for detector prototyping
then adopted as baseline solution

MAROC (Multi Anode Read Out Chip)

Originally designed for ATLAS



- 240-pin
- 16 mm^2

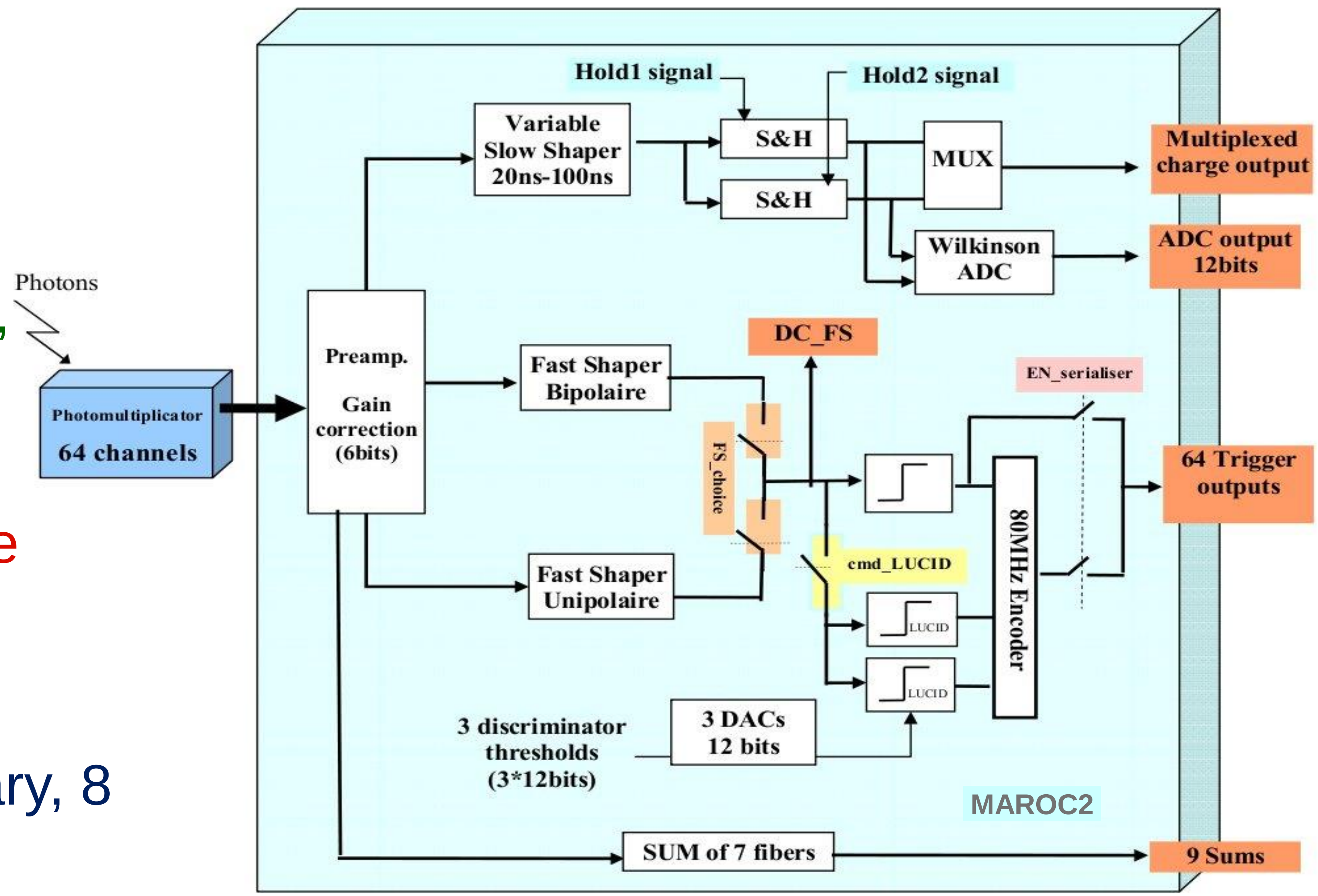
Single Channel (x64)

- Preamplifier, configurable (gain 8 bit)
- ★ Fast line: 25 ns shaper + discriminator ⇨ Binary datum
- ★ Slow line: 100 ns shaper + mem. cell + ADC ⇨ Analog charge
- ★ Prompt Sum line: send to one of 8 embedded sum output channels

PROs: 64 chs, designed for MAPMT, existing expertise, low power

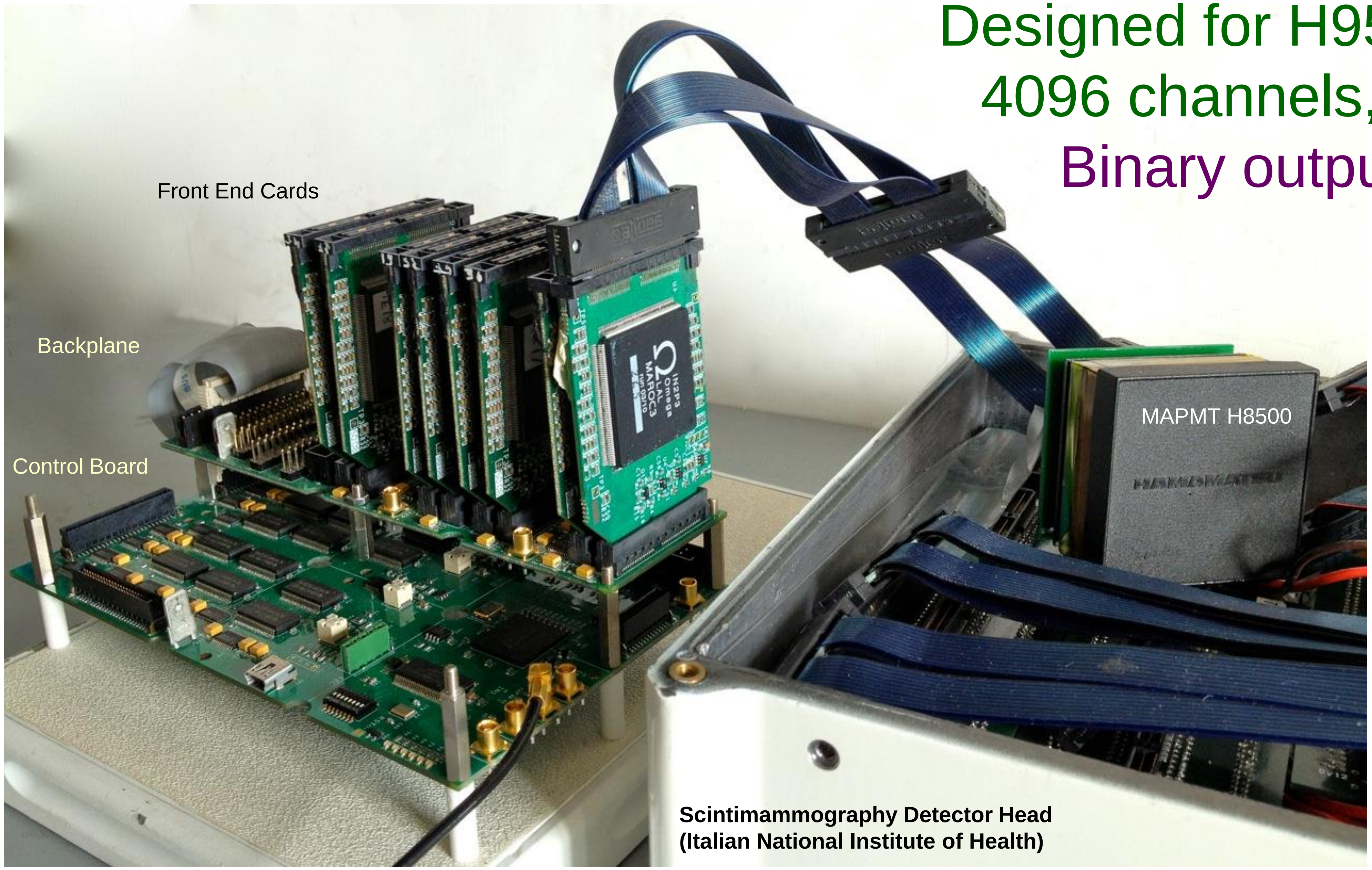
CONs: Analog limited latency, single channel time resolution few ns

Outputs: 1 Analog (MUX), 1 digitalized charge, 64 Binary, 8 prompt analog sums



In House MAROC based DAQ

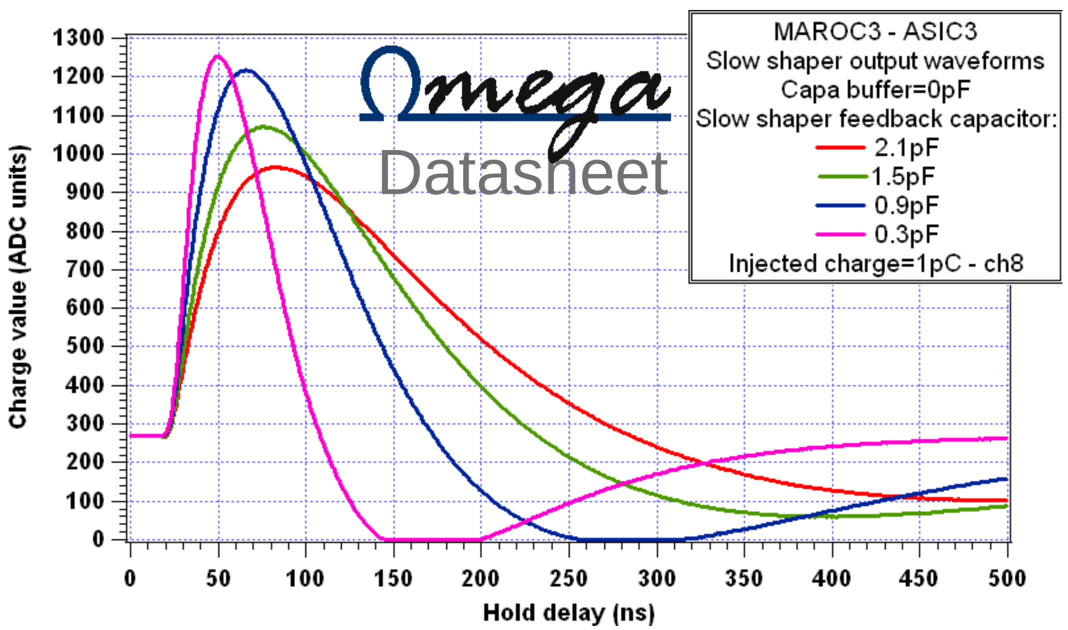
Original system developed for Medical Imaging with radionuclides
Many optical photons applications
Designed for H9500/H8500 PMTs
4096 channels, USB2.0 readout
Binary outputs for self-trigger



Not optimized for Single Photon and/or external trigger

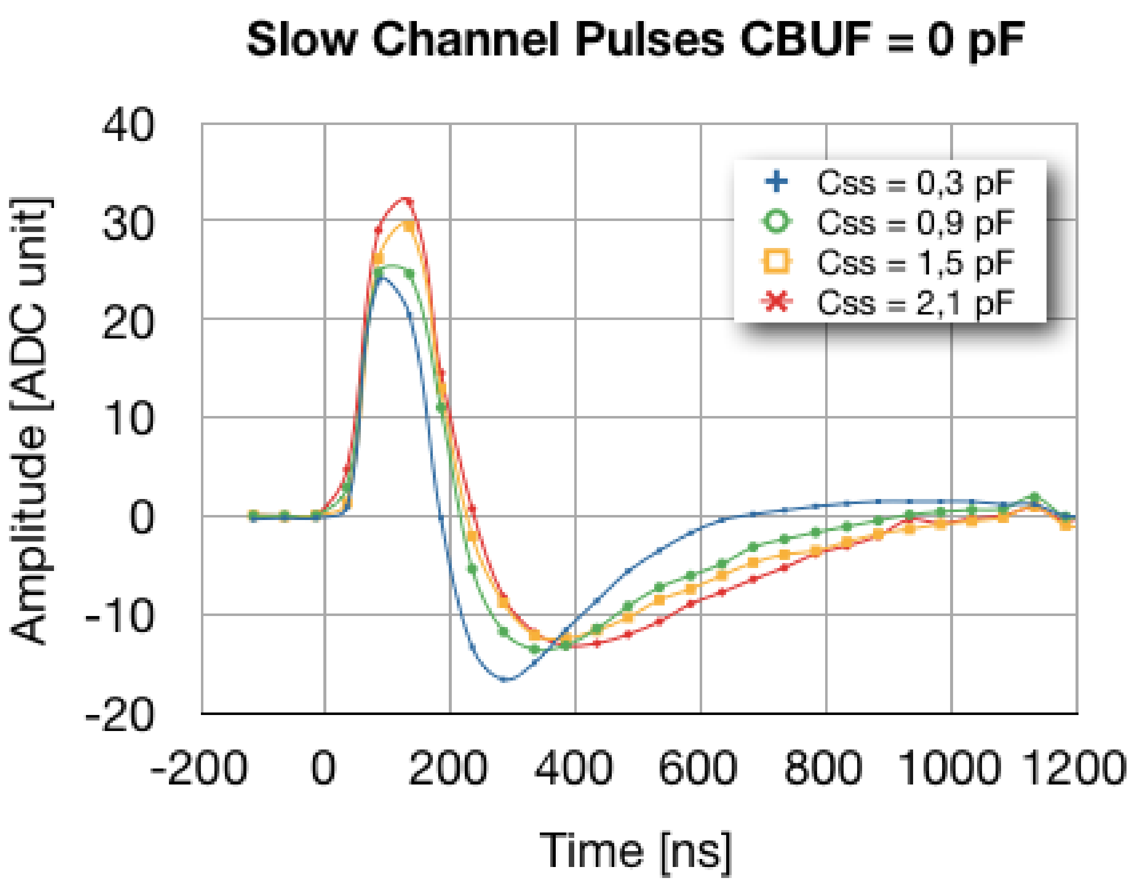
Modular design (FrontEnd + Bus + ControlBoard + USB int.)

Analog Response (Charge info)

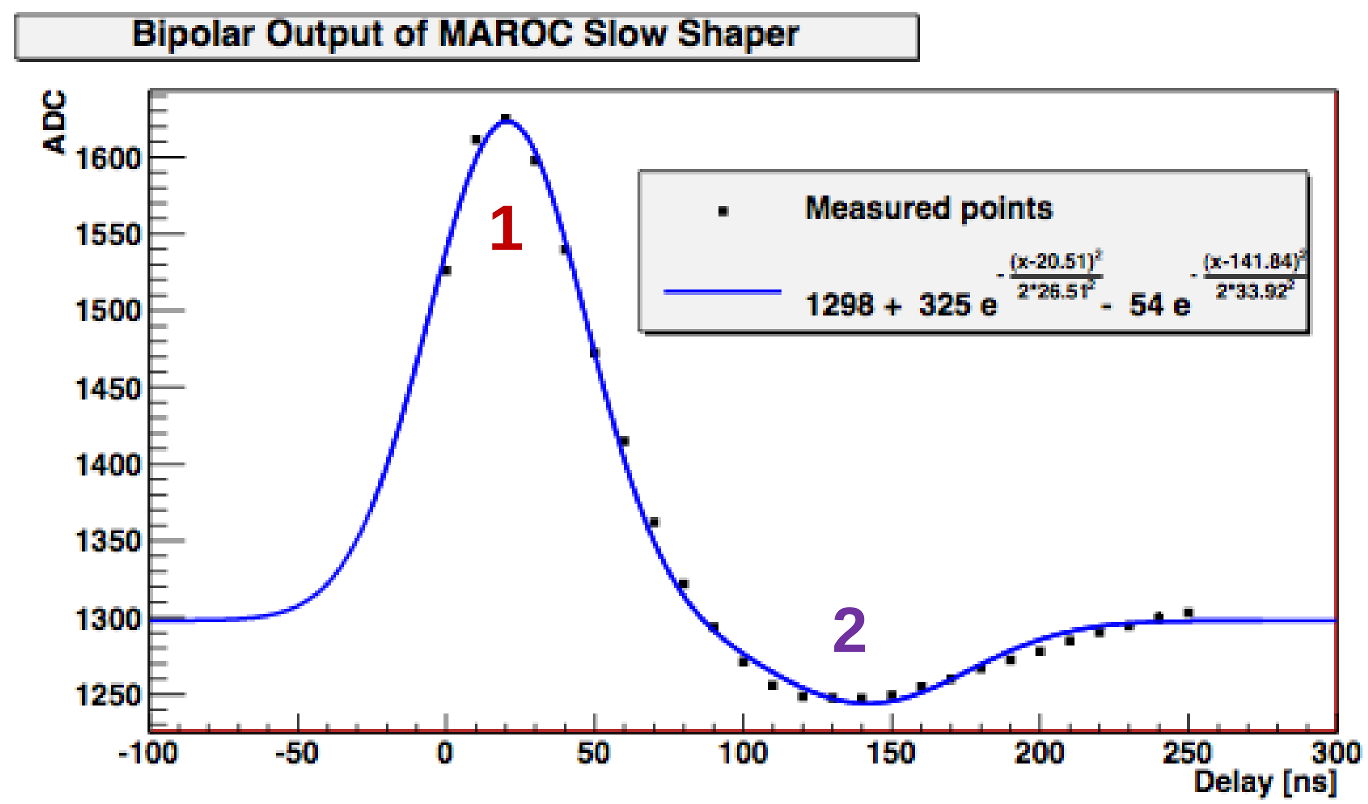


Bipolar analog signal offers two optimal sampling delays corresponding to the two local maxima:

1. positive, largest dynamics, occurs early
2. negative, additional 100 ns to trigger latency

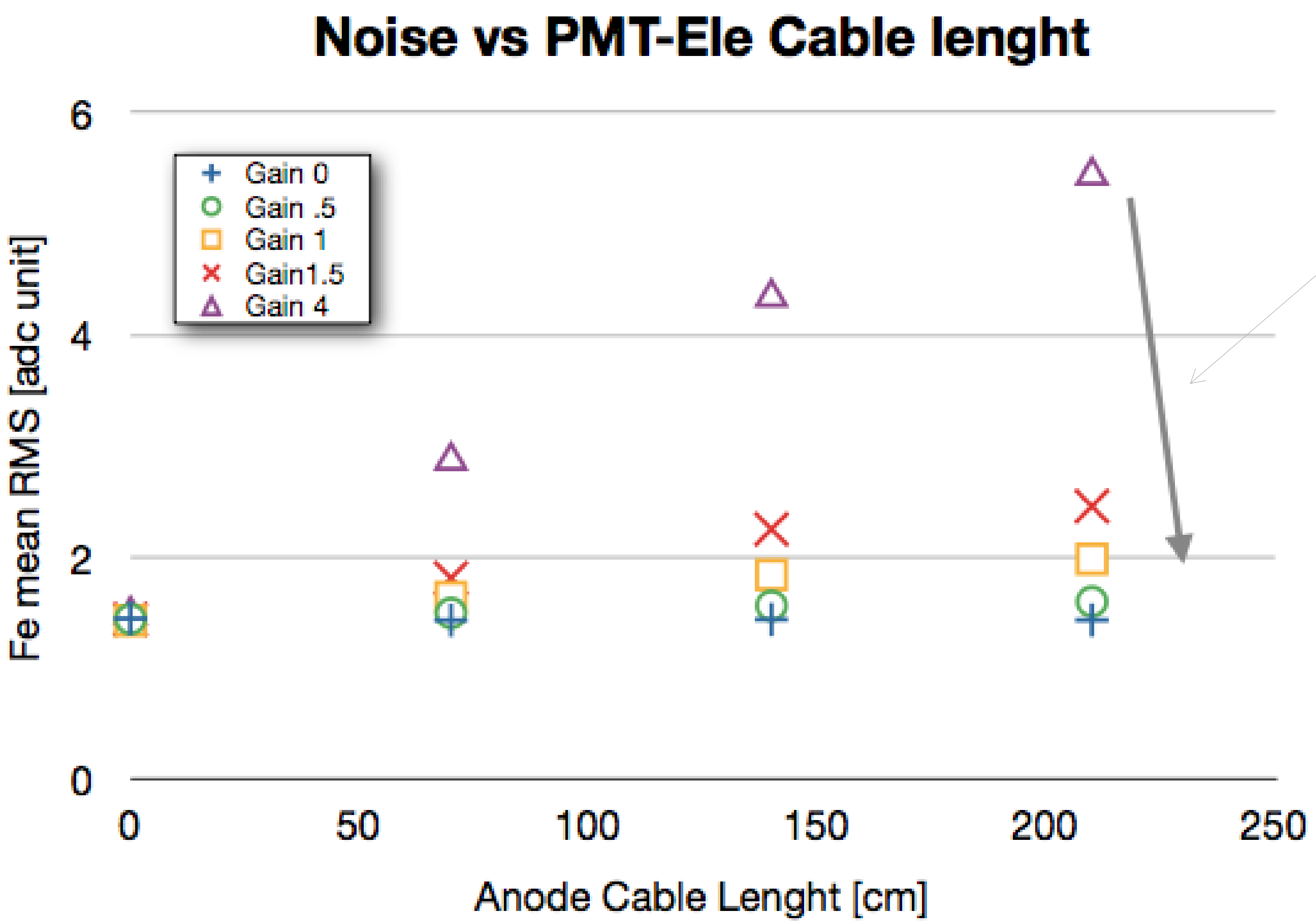


Waveforms well reproduced

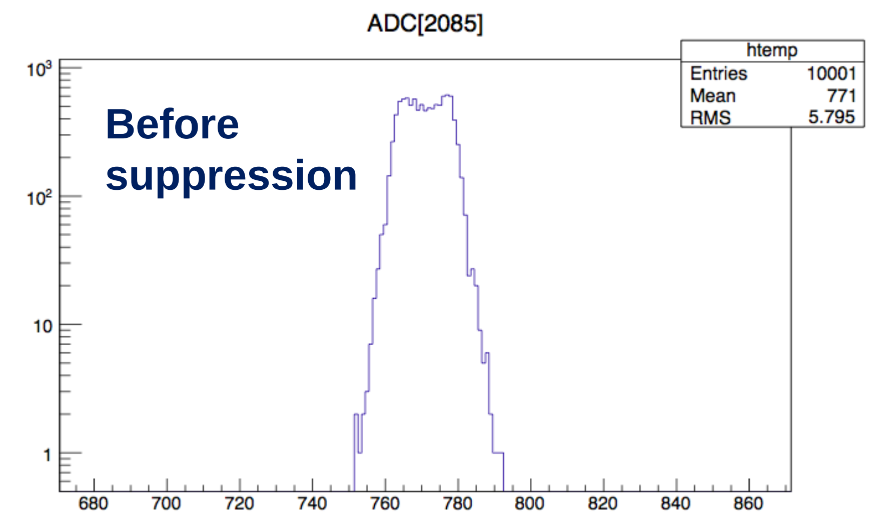


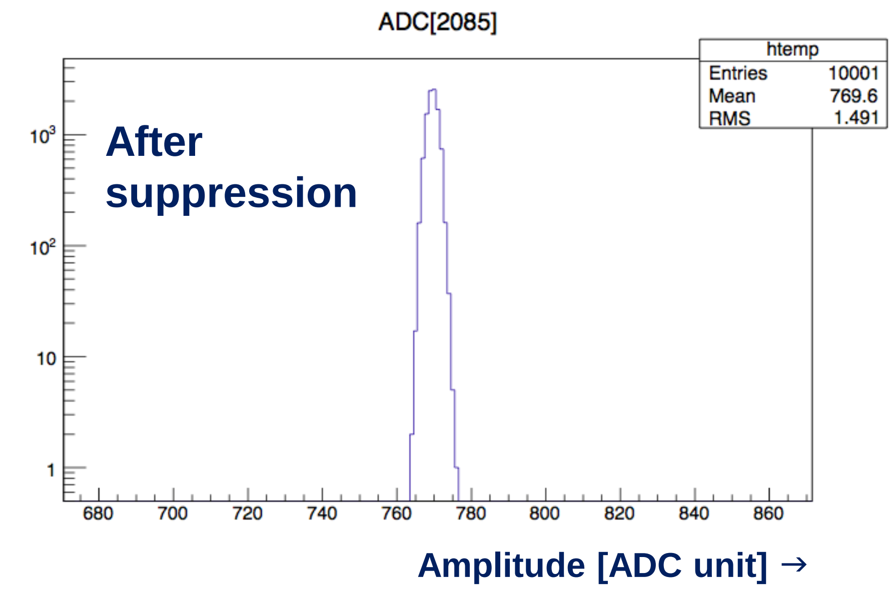
Dynamic Range Optimized (by ext. bias)
⇨ permit to reduce PMT operating HV

MAROC Analog Noise



Common noise suppressed offline significantly reduce the pedestal RMS





- COMMON NOISE seems to be the largest component
- Reduced or negligible noise with short or no cabling

! Noise conditions are site dependent !

MAROC from Analog to Binary

Mirazita Talk on Prototype Test

MAROC analog output worked pretty well in RICH prototype test, but cannot be used in CLAS12 due:
to limited latency (200 ns vs 8 μs required) and relatively slow readout

Single Photo Electron detection does not strictly need analog readout (e.g. HERMES RICH electronics)

⇓

MAROC binary information (64 parallel outputs) can be a valid alternative

C. Cuevas Talk on FPGA boards

- Binary data latency depends on external logic! Feasible
- Stability/sensitivity of threshold to single photoelectron? Tested
- Noise in MAROC fast (shaper) binary line ? Measured
- Readout Speed ? (not an issue) Estimated

Next slides

Single Photo Electron Level

External trigger / Light Source

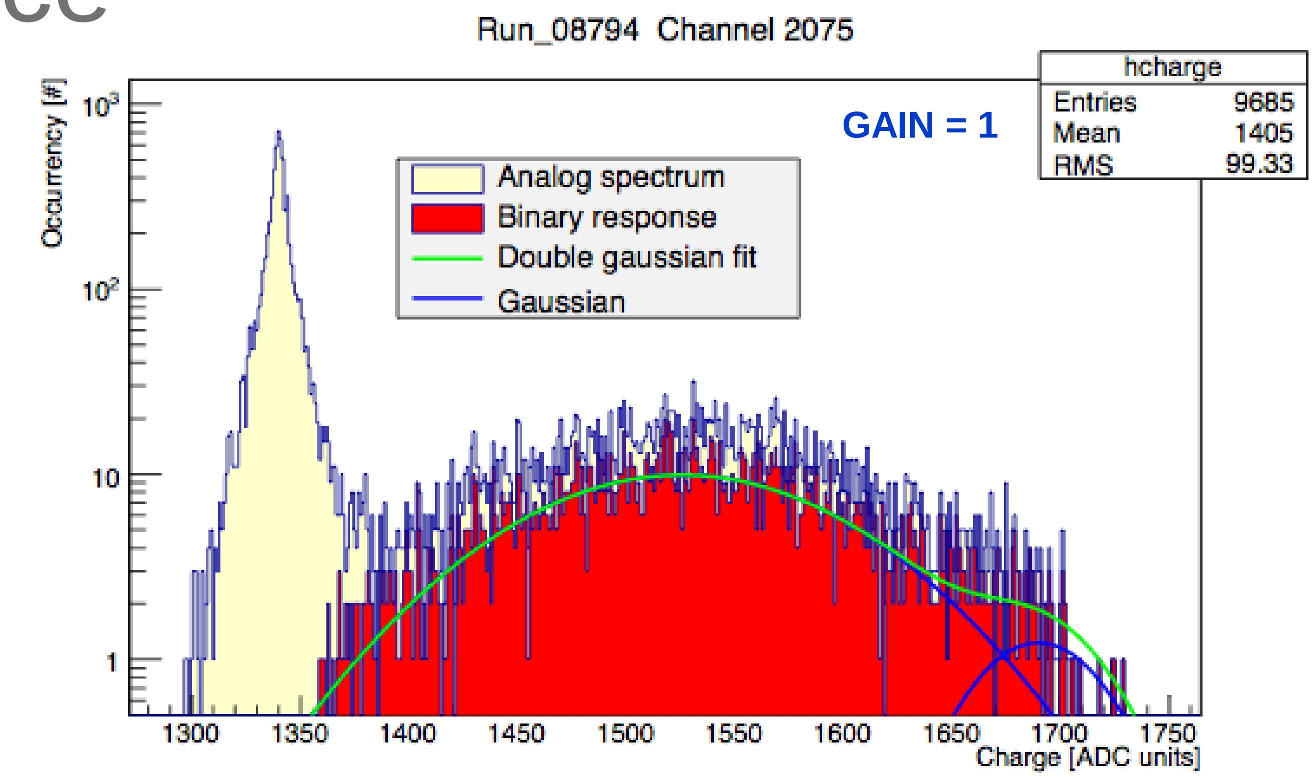
Clean SPE identification with binary data (red)

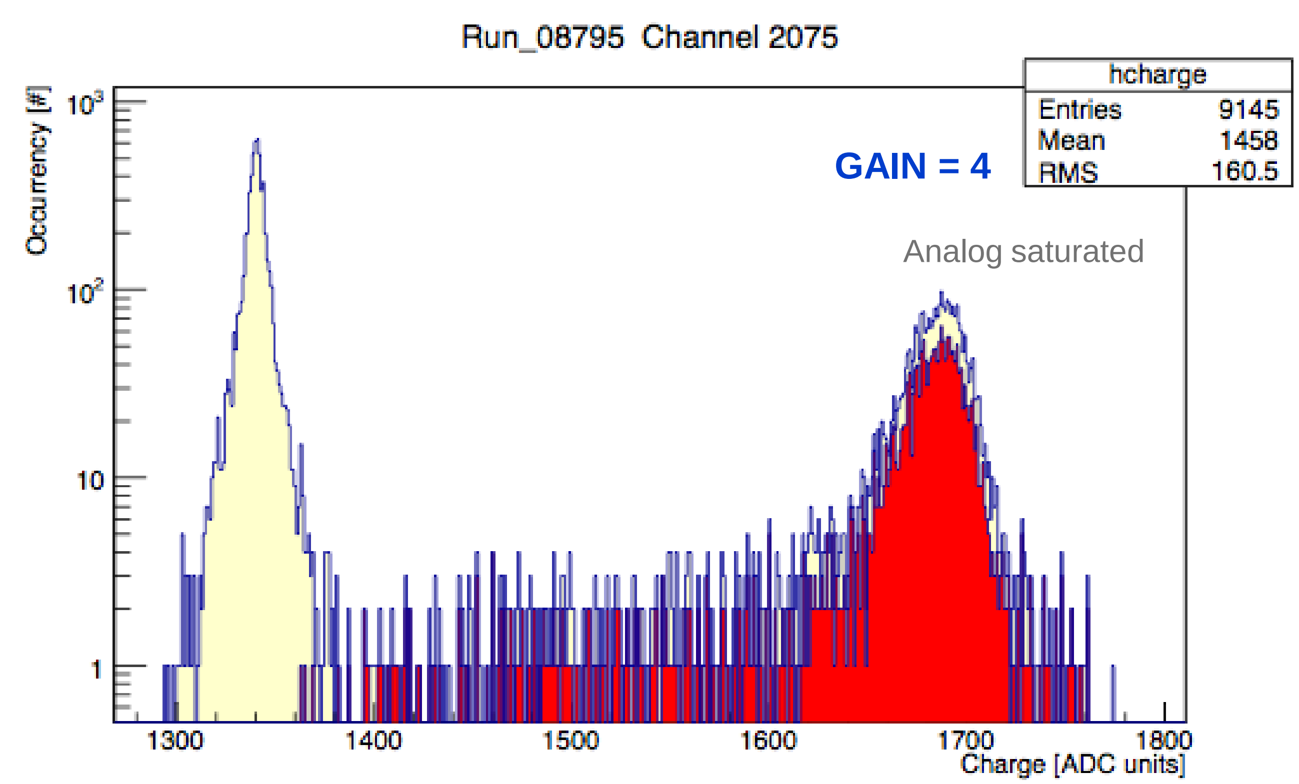
The smooth cut observed in the analog distributions can originate from:

- noise (both analog and binary combined)
- binary line provides better information on single photoelectron and «sees» good event below analog pedestal

Analog-binary amplitude mismatch due to not-optimal relative synchronization between analog and binary outputs (next slide)

Analog Timing: First local maximum





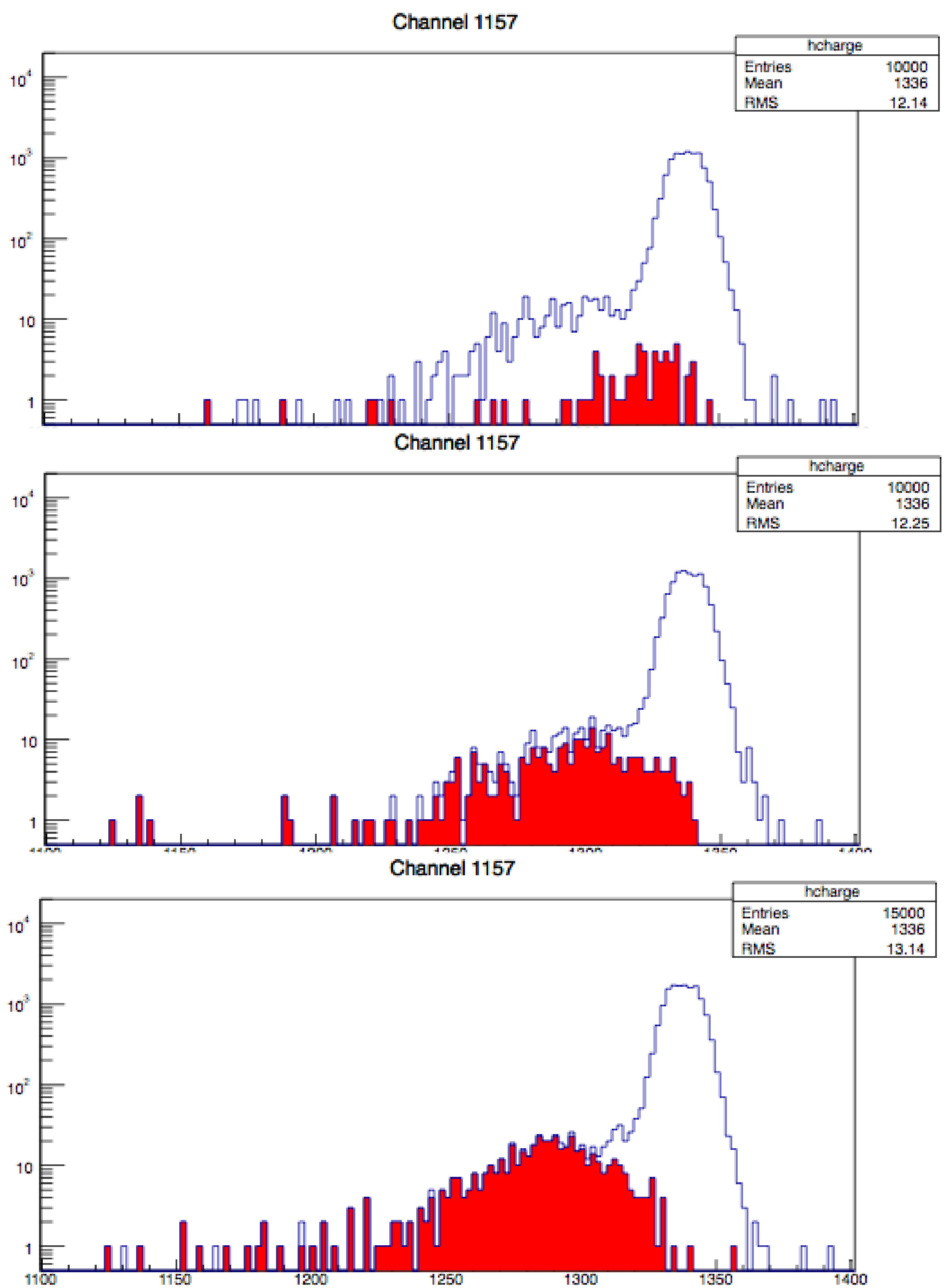
Binary output behaves as well as analog (or even better)

Single Photo Electron Level

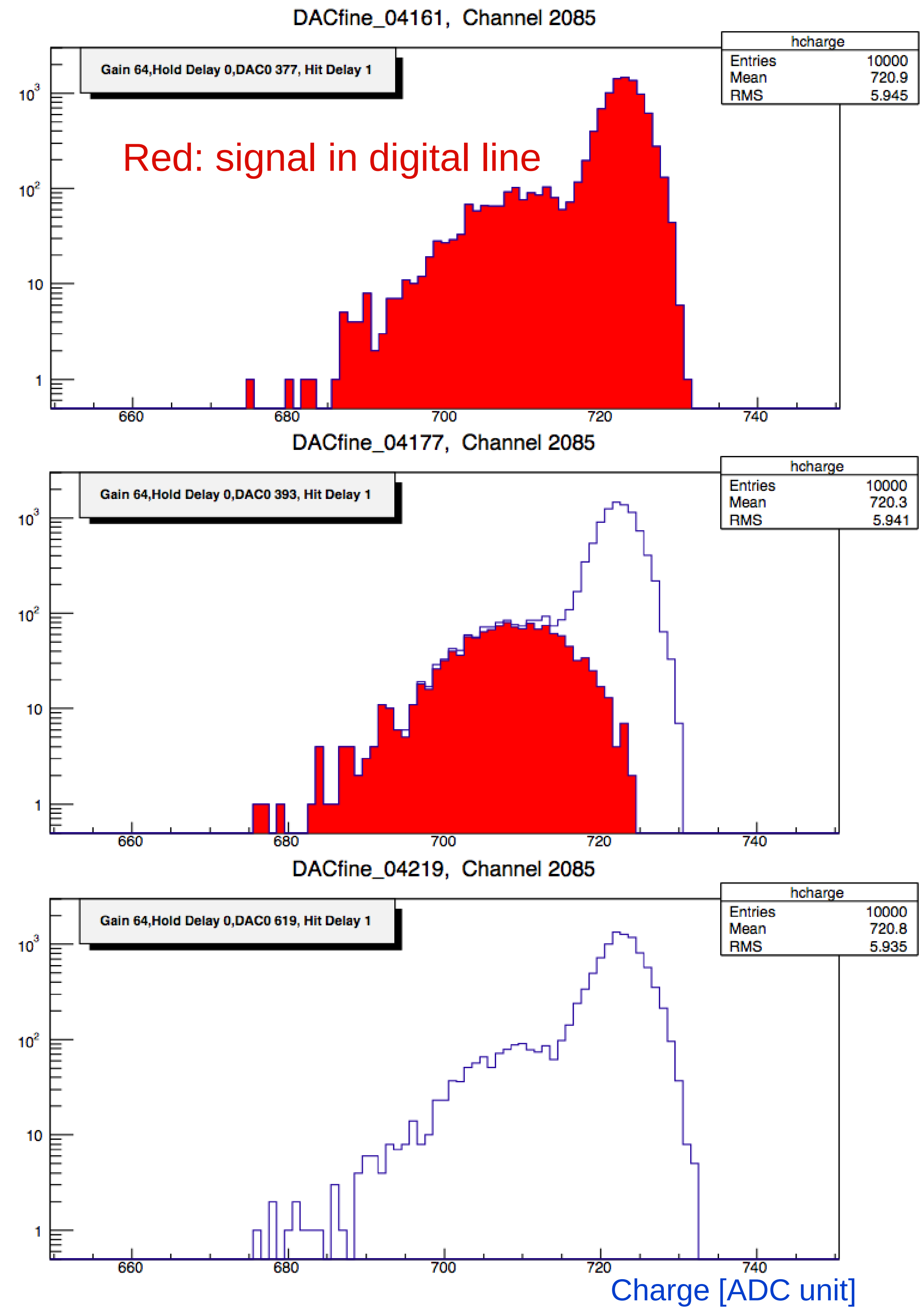
External trigger / Light Source

Common noise not subtracted

Analog-Binary relative synch (25 ns step)

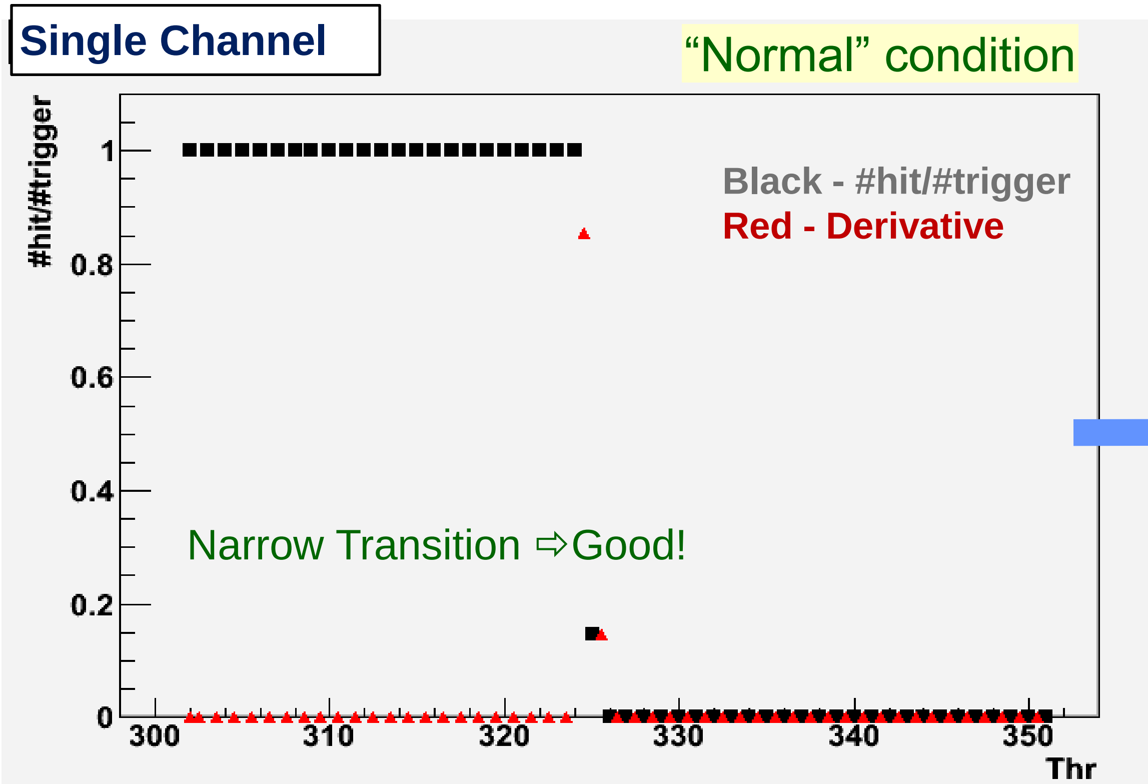


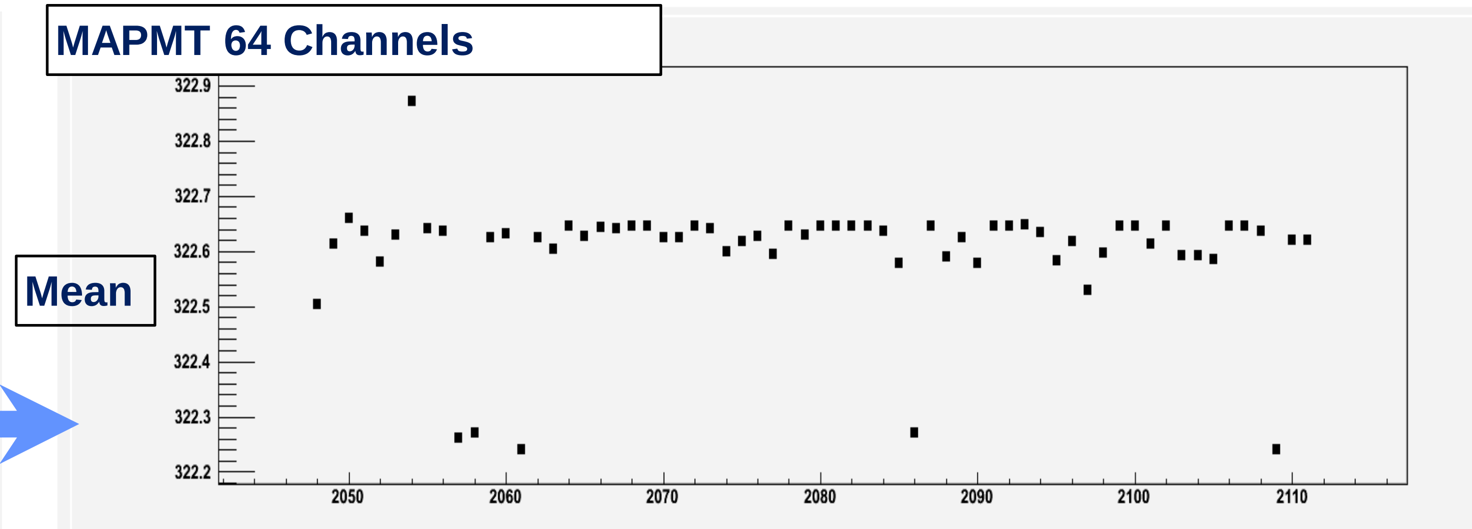
Binary Line Threshold (100 unit step)

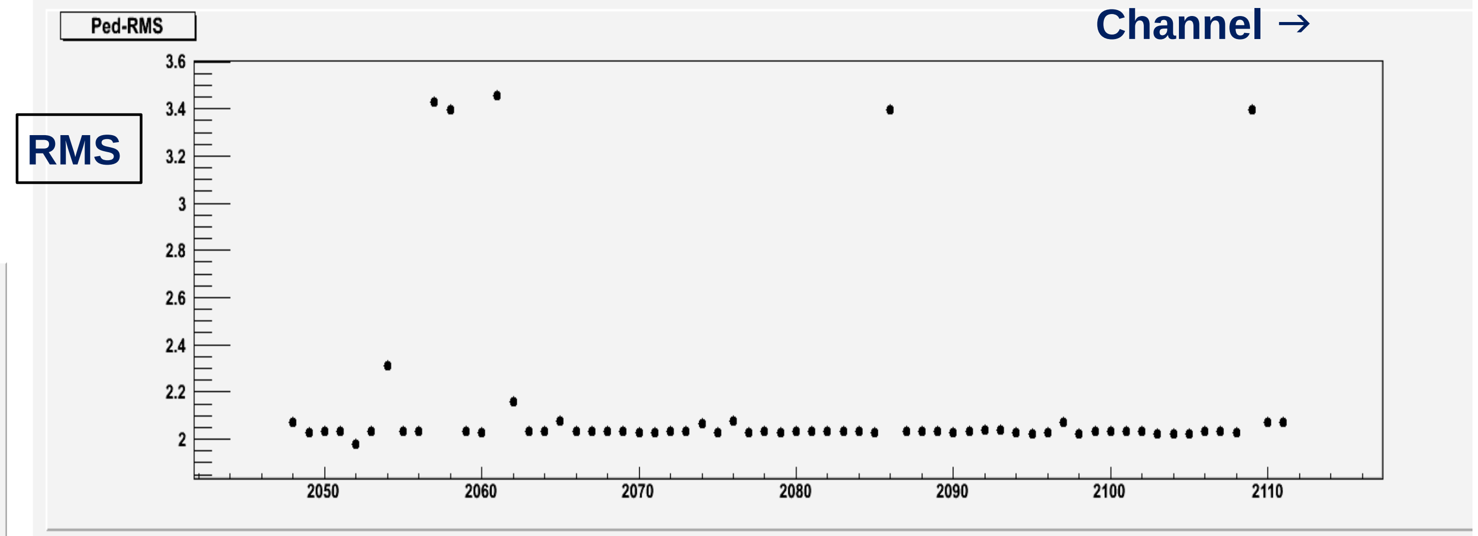


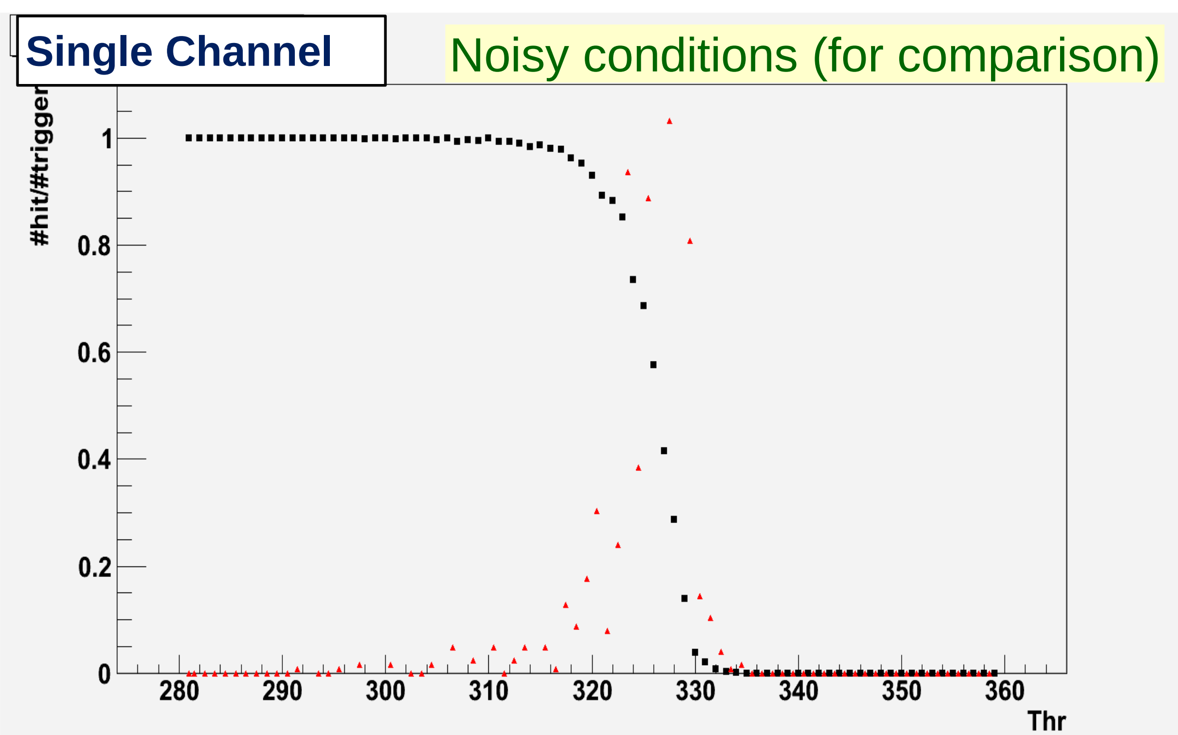
MAROC "Binary Noise"

Binary pedestal – Open inputs: No PMT connected









⇨ Digital RMS < 1 thr unit (<3mV)

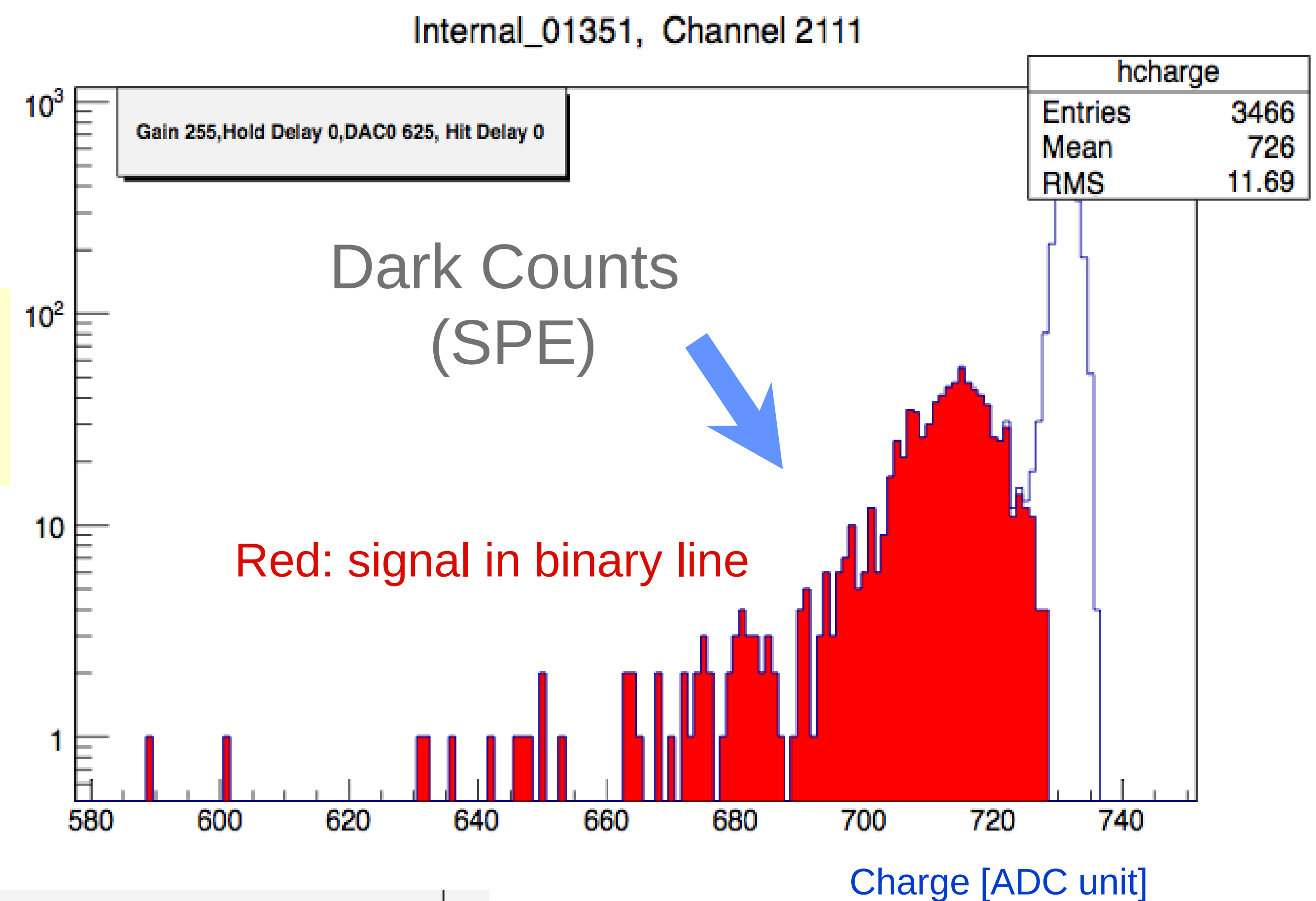
Analog Pedestal RMS 3-5 ADC unit (2-4 mV)

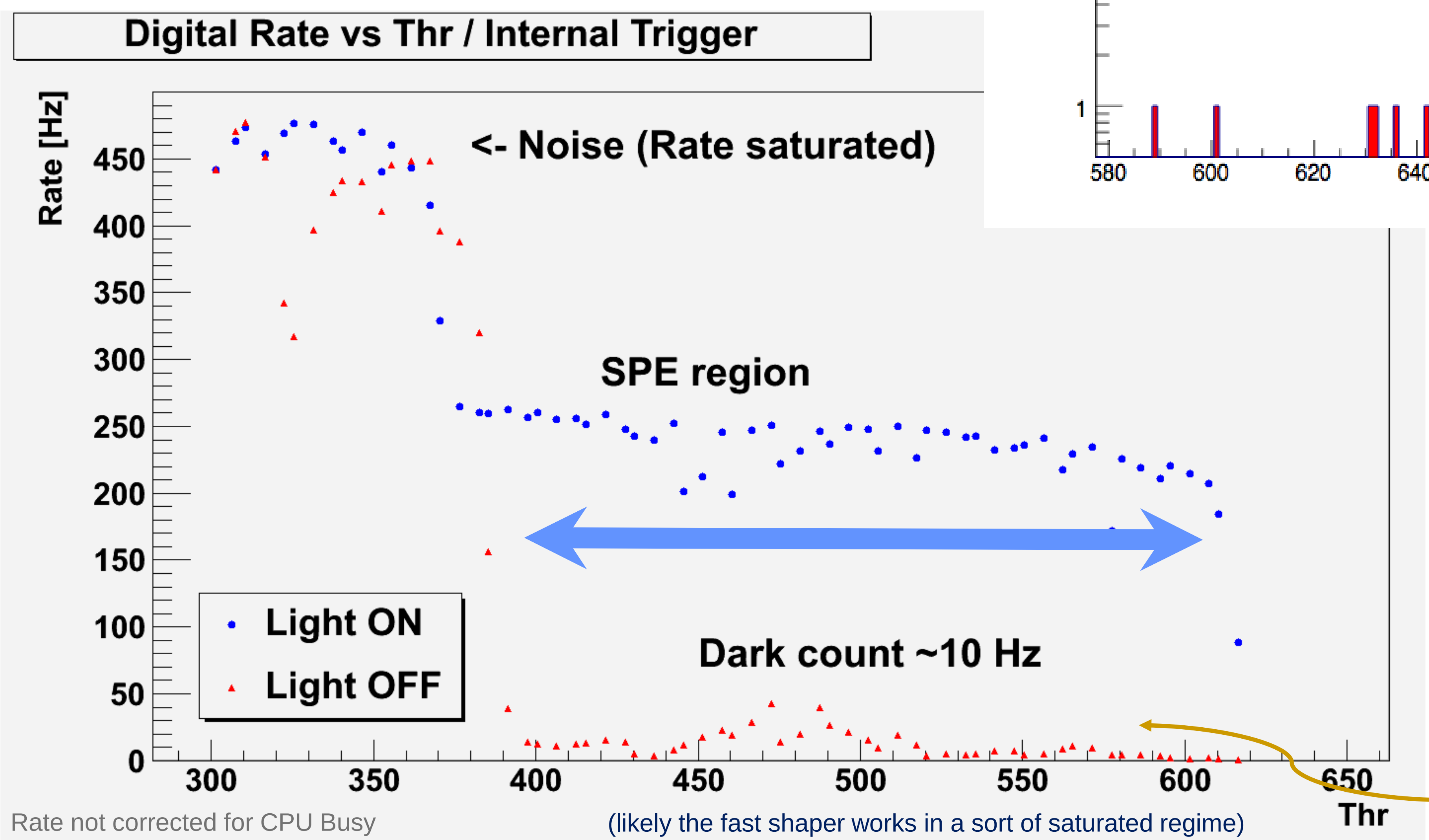
Digital/Analog comparable ⇨ see next for SNR

Dark Noise and SPE

Self-trigger

SPE region extends over ~200 thr unit
(compare with Ped_RMS <1)





"sharp" Gaussian cut, no pedestal raising

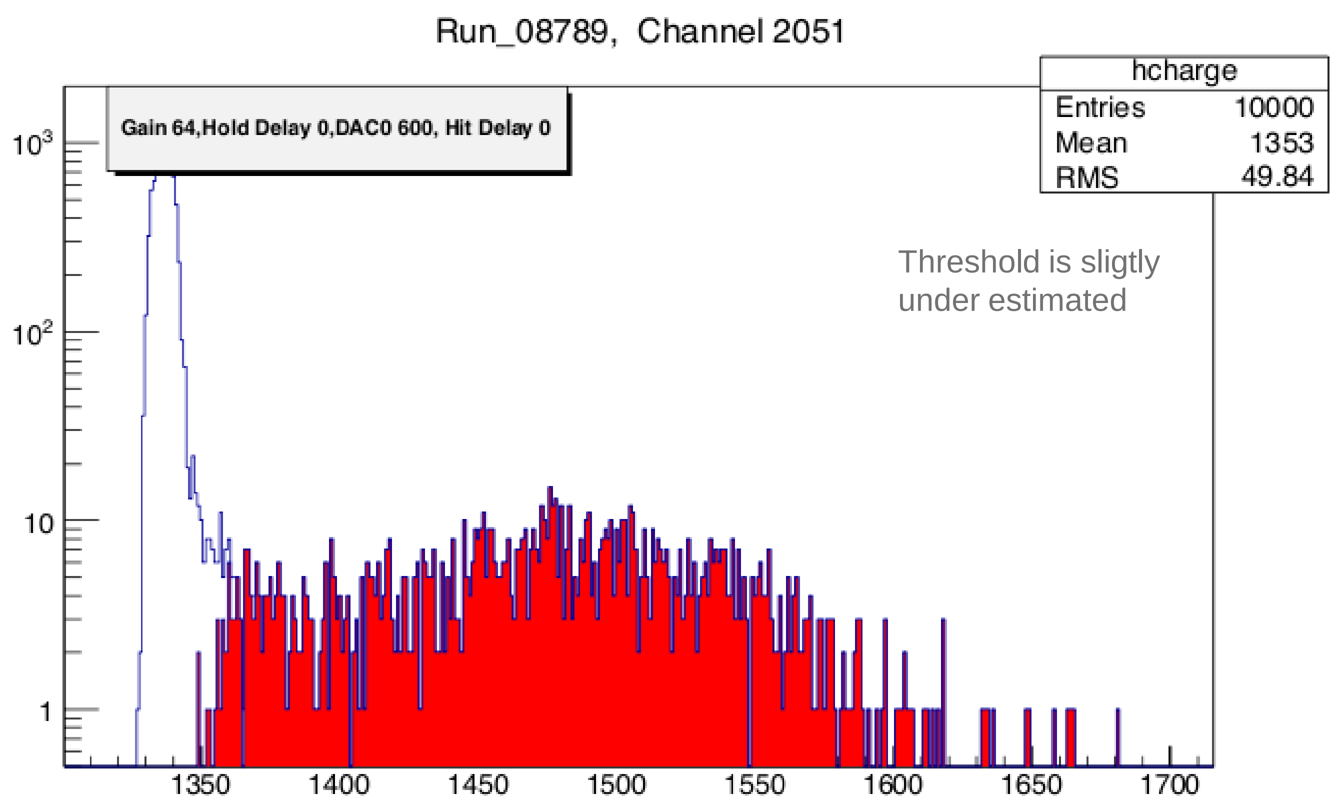
⇓

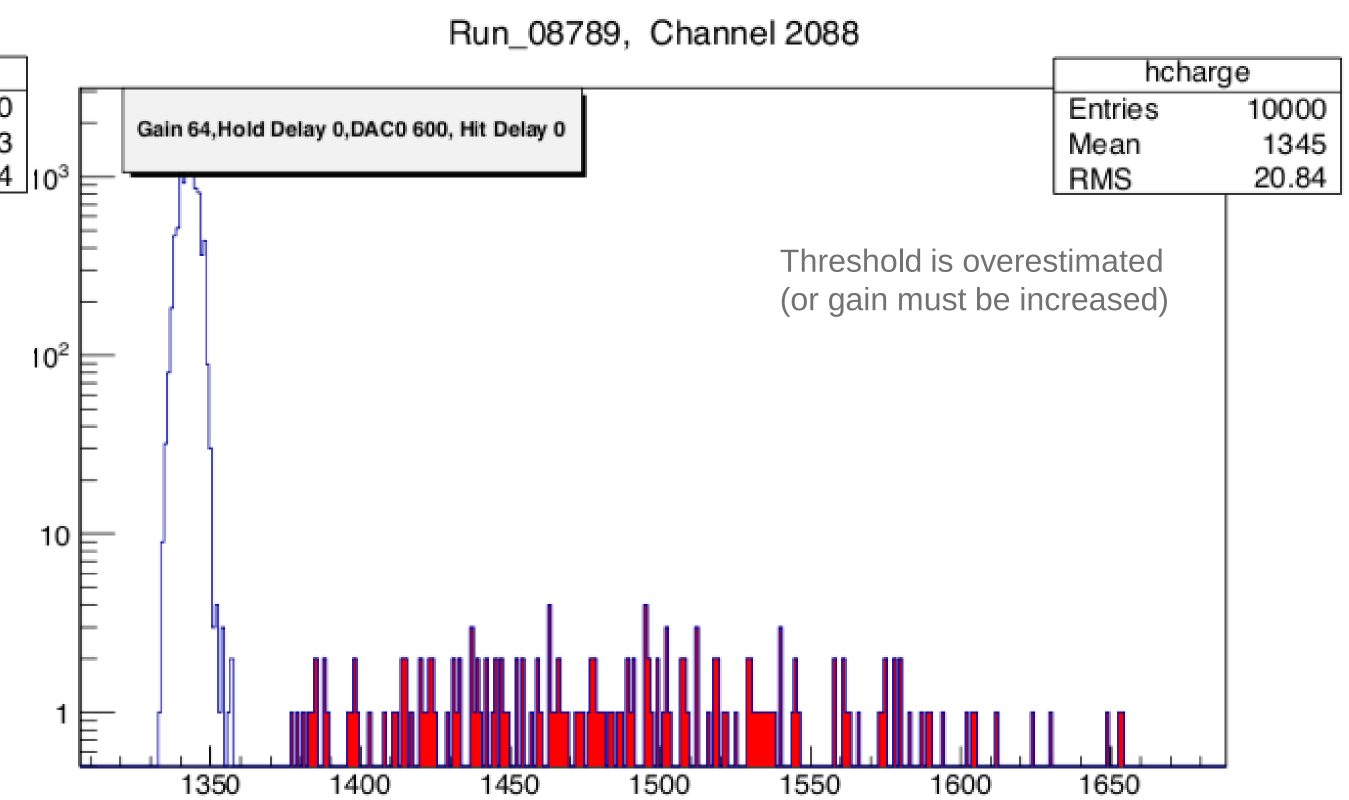
hint of better SPE separation than analog (?)

Dark rate consistents with MAPMT specs

Gain Equalization

Self-trigger capability can be exploited for effective calibration (gain equalization, threshold selection, MAPMT gain compensation)





Dark spectra for two different channels

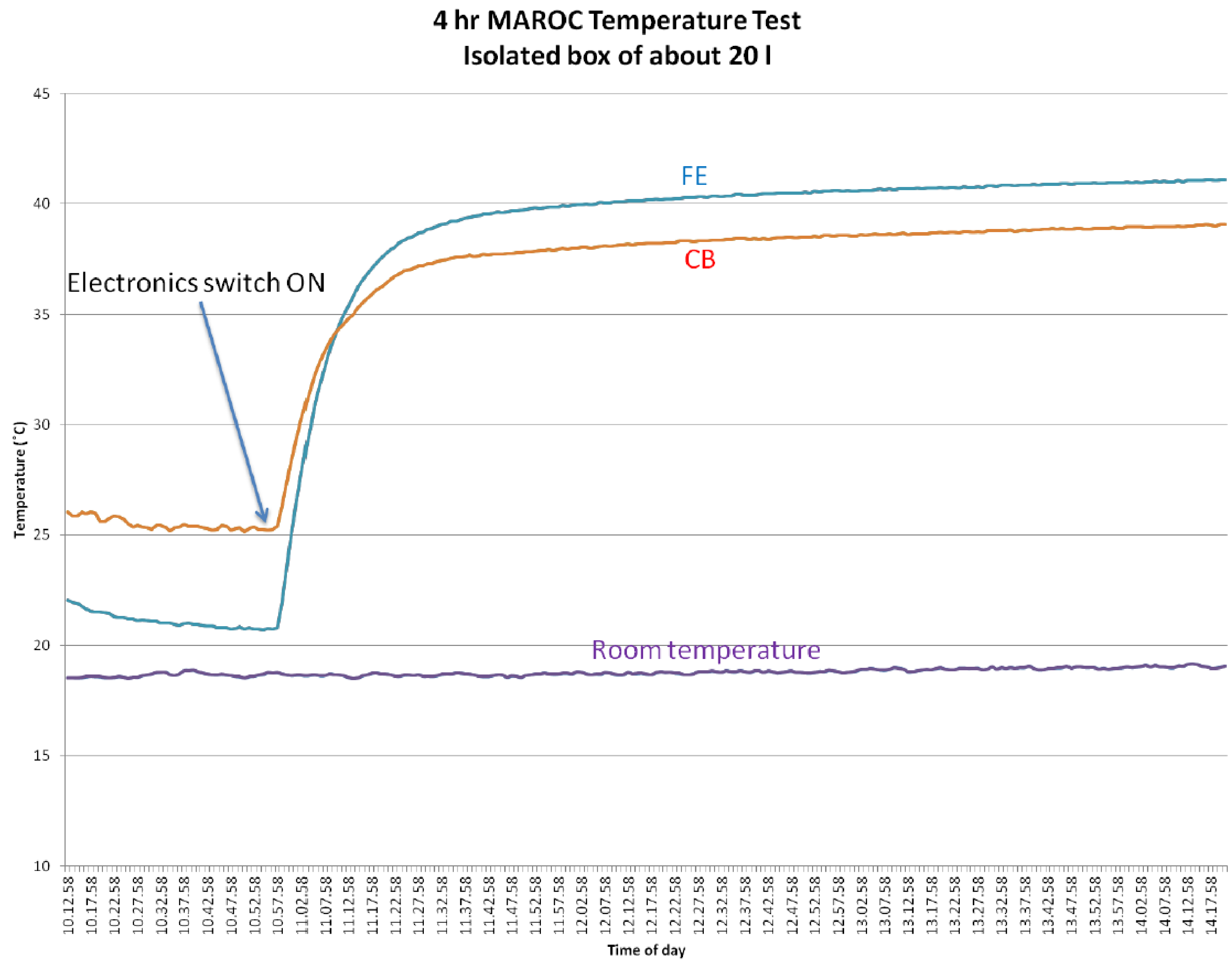
The small dark count rate (10Hz) is quickly acquired in self trigger mode, while in external trigger would require either a long acquisition time or an external light source.

MAROC Front End - Heat dissipation

- MAROC power consumption as small as 3.5 mW/ch
- Current implementation at the level of 0.5 W/card → total power for 400 cards is **~200 W**

- First thermal test with 8 FE + 1 Controller in sealed container of 20 liters volume – no cooling.
- Two probe points: contact with Front End (FE) and close to the Control Board (CB) – «hottest positions»

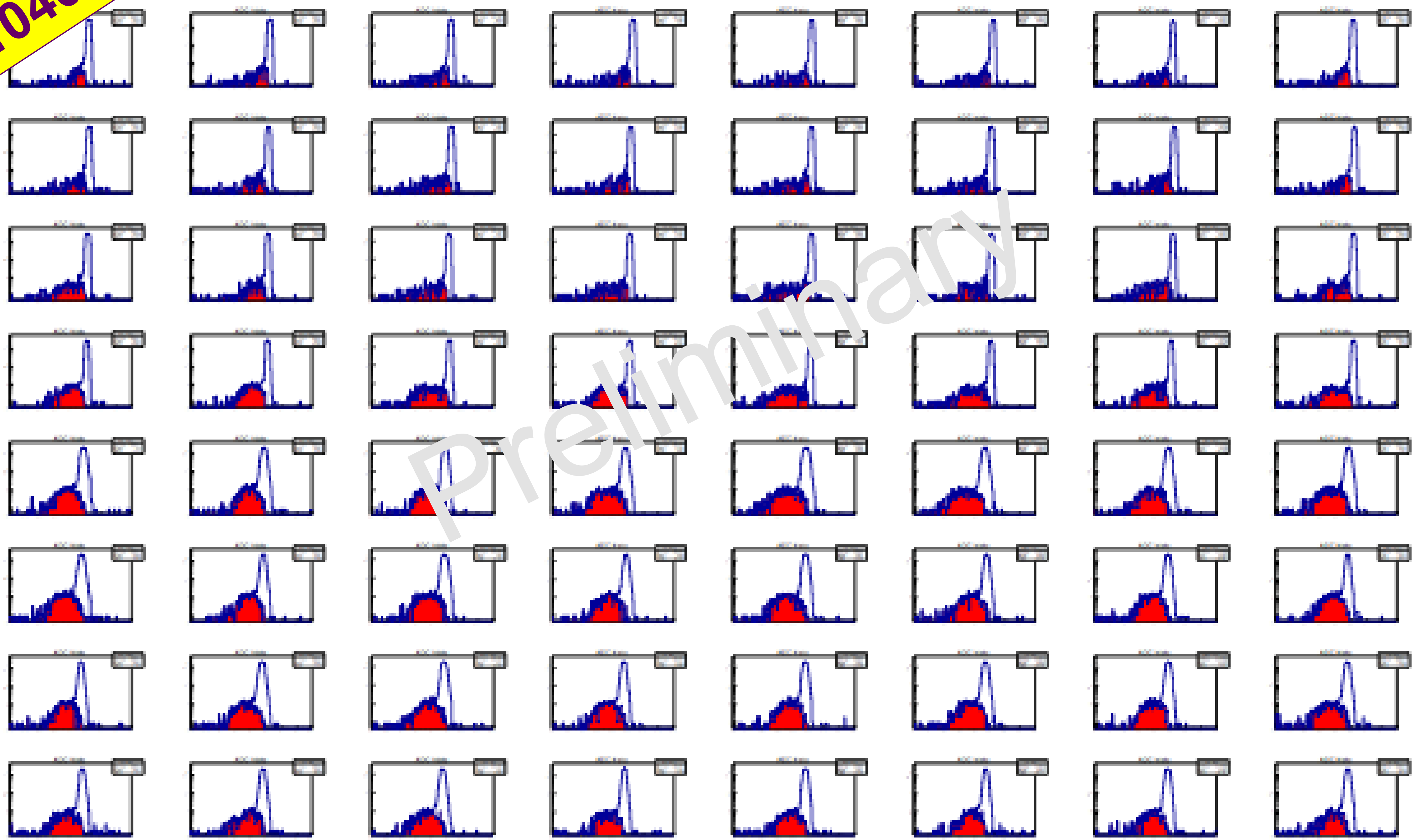
- Small temperature increase **~ 1°C/h** in running conditions (after initial rump up) **~ 40 °C**



Small fresh air flow in electronics housing expected to be enough to keep stable conditions

Cherenkov Light (BTF Test Aug/2013)

HV=1040 V



Online display from MAPMT analog spectra with binary response

Small arc of the Cherenkov ring is clearly visible

New MAROC based ASIC board

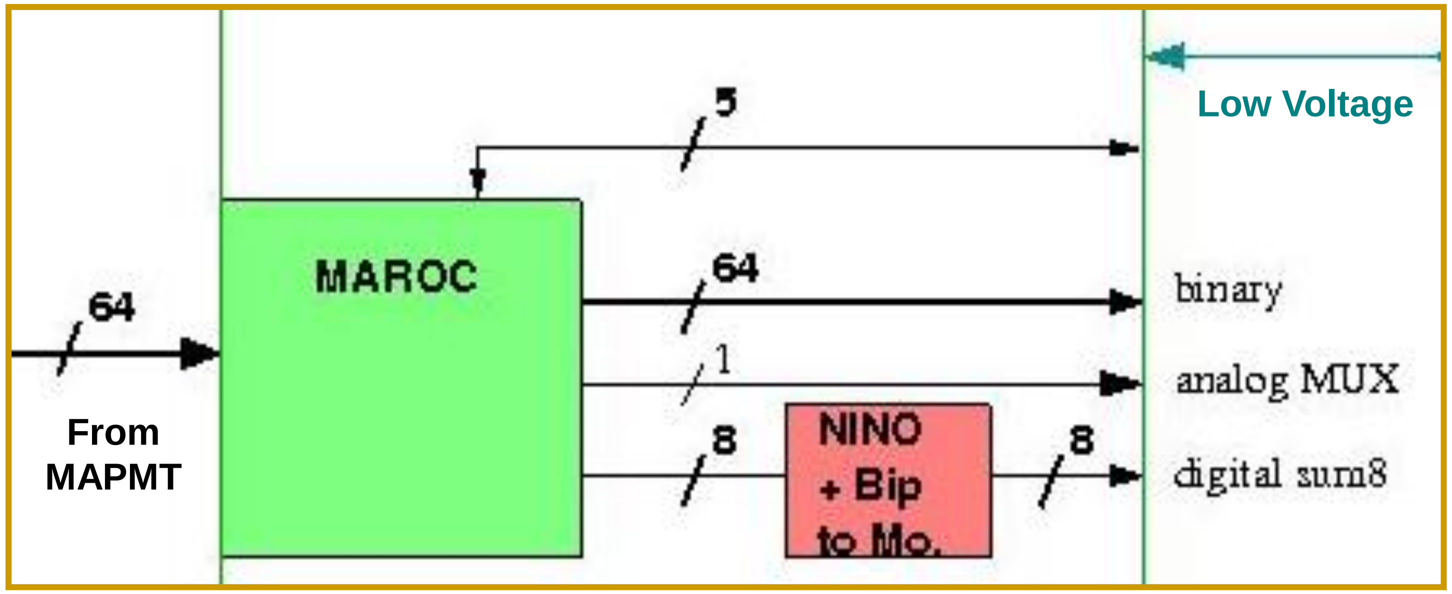
The existing electronics not suitable for CLAS12 RICH operation:

- not optimized for binary readout,
- limited speed through USB-2 interface,
- layout requires cabling to connect MAPMT
- no time information

Need to implement a <u>new front-end board</u>

(reuse large part of existing design)

- Directly connected to MAPMTs (no cables): one MAPMT ⇔ one MAROC
- 64x parallel binary outputs as main information
- 8x analog sum8 sent to fast amplifiers and discriminator (NINO from CERN/ALICE) for sub-ns timestamp resolution
- 1x analog MUX (or the internally converted digital charge) for calibration (event by event or dedicated runs)

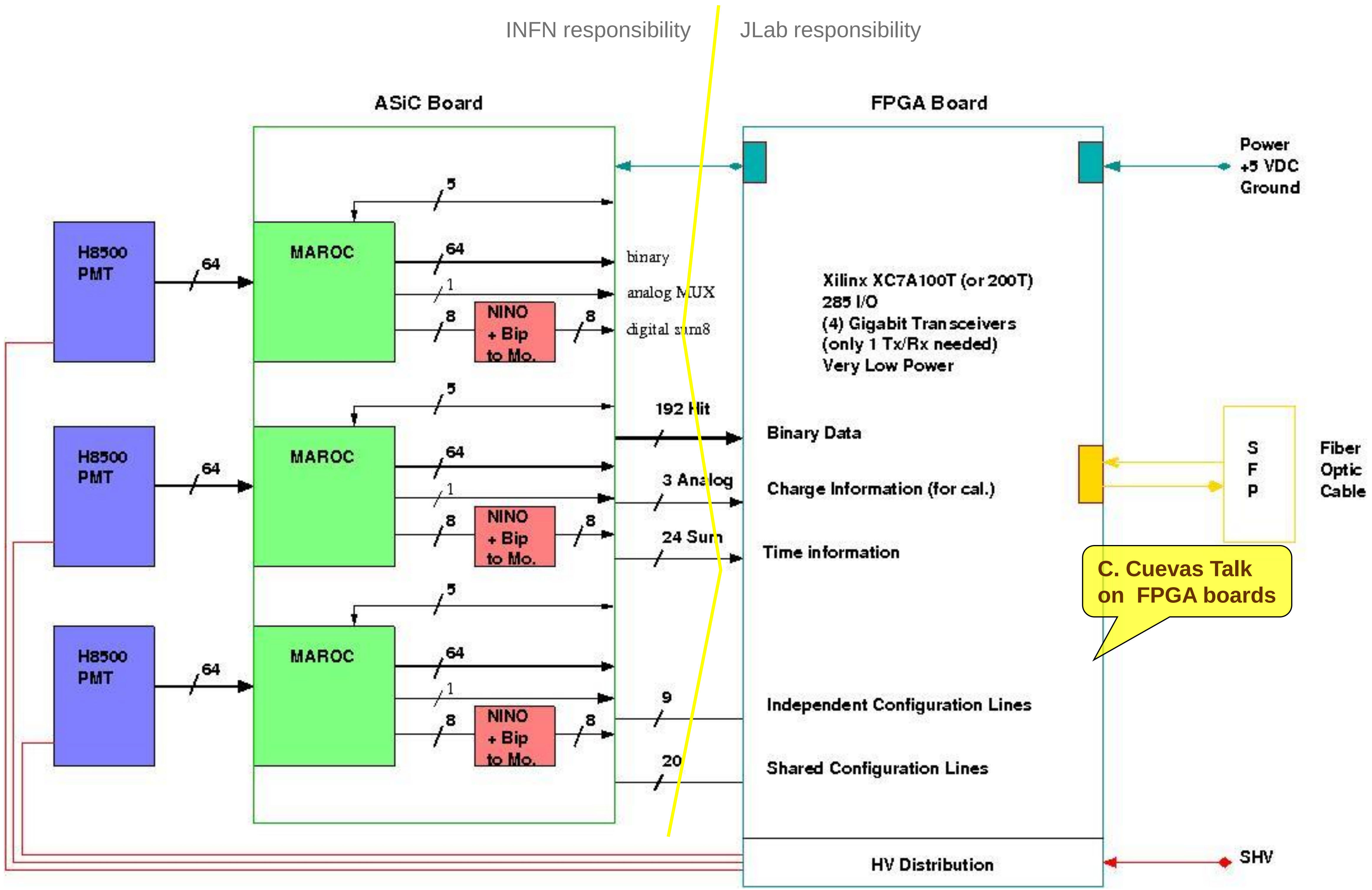


73 outputs lines

23 configuration lines (20 shared with other MAROCs)

Few options (not exclusive) open for calibration/stability checks

DAQ electronics



Modular design with 3 logic/physical layers
(similar approach of the existing electronics ⇨ straightforward porting)

Readout Speed and Dead Time Estimation

- When a binary channel has a hit the corresponding time is stored in **13 bits** (1 ns resolution and > 8000 ns time range); 6 bits for addressing
- Each MAROC sum line has **14 bi**ts information (0.5 ns resolution, same time range); 3 bits for address
- Charge info for one channel, calibration/stability check (12bits ADC)
- Maximum hit occupancy **10%** (exagerated! one order of magnitude larger than GEANT4 Simulation)
- MAROC multiplexing factor **3** (up to 3 MAROCs share the same optical link)
- Fast **2.5 Gbps** serial link (assume 2 Gbps sustained)

Expected Readout Time (from MAROC to SSP):

[(19 bits x 64 channels + 17 bits x 8 sums) x 0.1 occupancy + 12 bits]

x 3 MAROC/board / 2 Gbps

= ~220 ns

or <0.5% dead time at 20 kHz

Negligible!

Time data words can be further compressed in FPGA

Requirements fulfillment

Single photoelectron sensitivity	~50fC	Specs, slides 9, 10, 12 ...
Number of channels per sector	25600	64ch/ASIC adequate
Anodes gain spread compensation	1:4	Specs, slides 4, 13
Event Rate	20 kHz	Slide 16, 17, 18, Cuevas talk
Dead Time	few%	
CLAS12 trigger latency	8 μs	Slide 16, 18, Cuevas talk

Time resolution ~1 ns

To disentangle direct and reflected photons (can be done off line)

Specs, slide 16

Compactness/ Power consumption

Max area 1 m^2, max thickness 10 cm, power compatible with air flow heat dissipation

Specs, slide 14

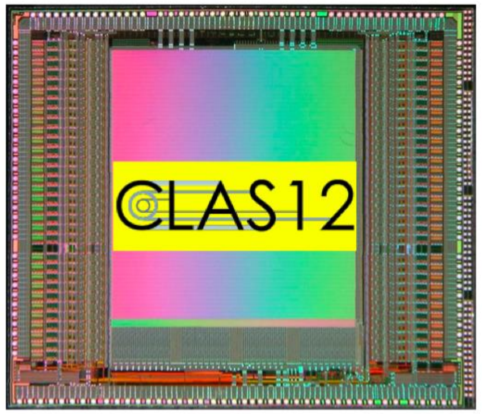
Radiation hardness

Must operate in the same irradiation level of the MAPMTs

MAROC build in CMOS 0.35 μm for ATLAS radiation conditions.
No surprise expected

Alternative / DREAM ASIC

Dead-timeless **R**eadout **E**lectronics **A**sic for **M**icromegas



Single Channel (x64) - Design for Micromegas @ CLAS12

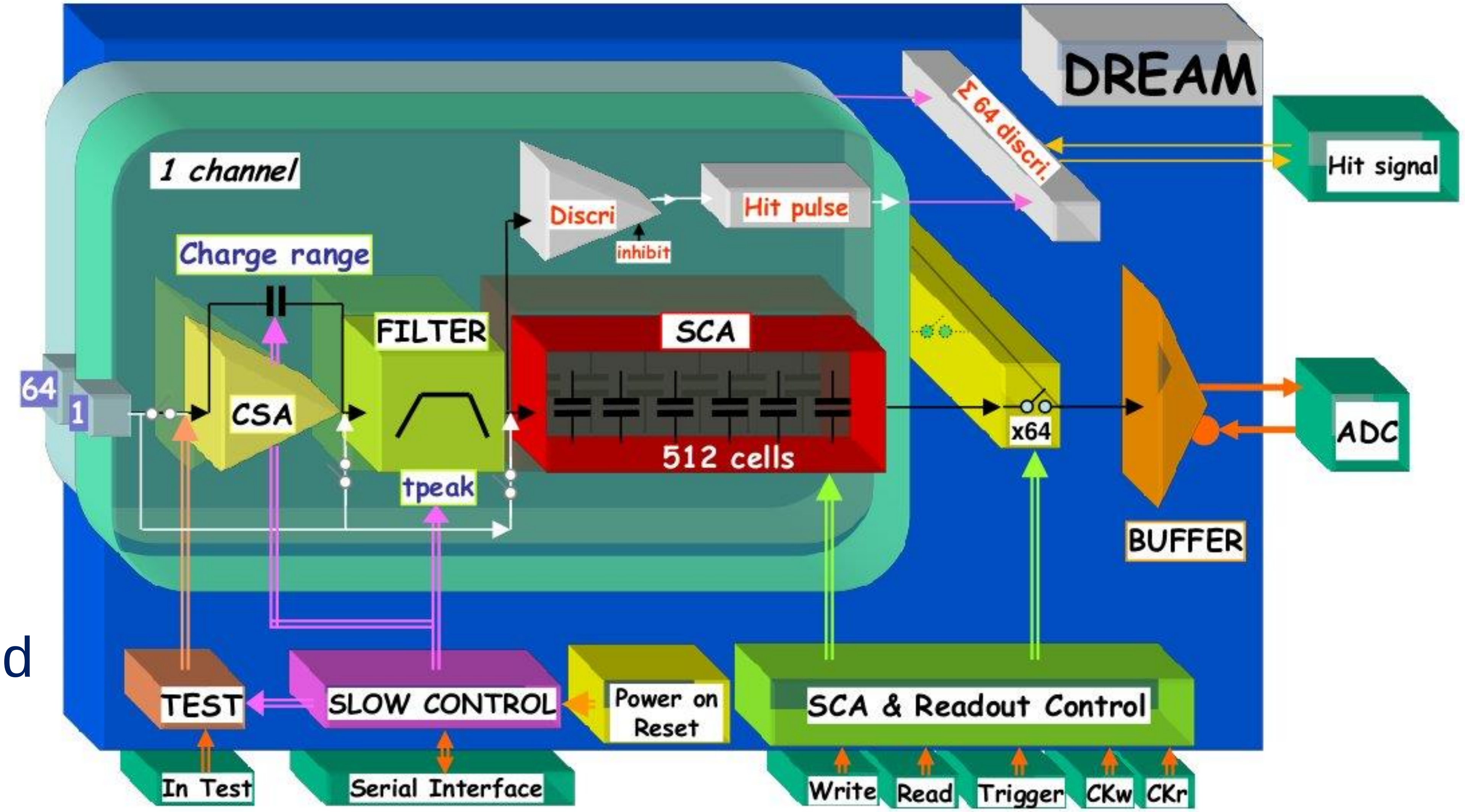
- Preamplifier, adj gain on 4 ranges (60fC,120fC,240fC,1pC)
- Shaper, adj peaking time 16 values from 50 ns to 1 µs
- Analog memory 512 cells, sampling rate 1-50MHz
- Discriminator, trigger pipeline 16 µs , sum of 64

- 140-pin
- 0.4mm package,
- 17mm x17 mm footprint

PROs: analog pipeline, designed for JLAB12

CONs: dynamic range (?), time resolution

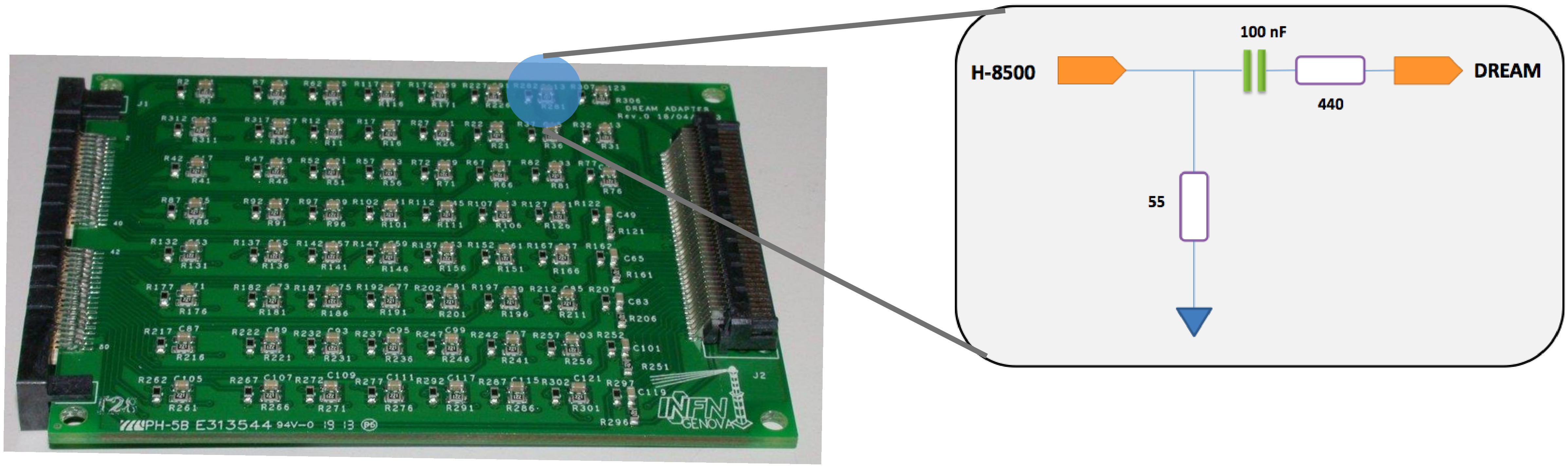
Output: Analog MUX and Digital Sum



PMT DREAM interface

Dead-timeless **R**eadout **E**lectronics **A**sic for **M**icromegas

R&D from Micromegas group



Attenuation board for H8500
with various divider ratio for testing

TEST SCHEDULED 2013 October at INFN-FRASCATI

Conclusions

- MAROC chip (binary data) represents a valid choice for RICH readout
  - ✓ **Laboratory/Beam tests showed a clean SPE detection**
- Porting of current MAROC electronics in CLAS12 DAQ framework expected to be reasonably simple
  - Time measurement will be the really new aspect
- DREAM option left open (till test on PMT coupling Oct/2013):
  - Provide multi-sample analog information
  - Synergy with current development for microMeGas
  - Expected easier maintainance (both HW and SW)
- Next steps:
  - continue analysis of BTF data,
  - finalize MAROC test (internal ADC, timing),
  - DREAM test,
  - design the new front-end board for the RICH and start testing it.

End