Test of APV25 on FEE board for GEM detector

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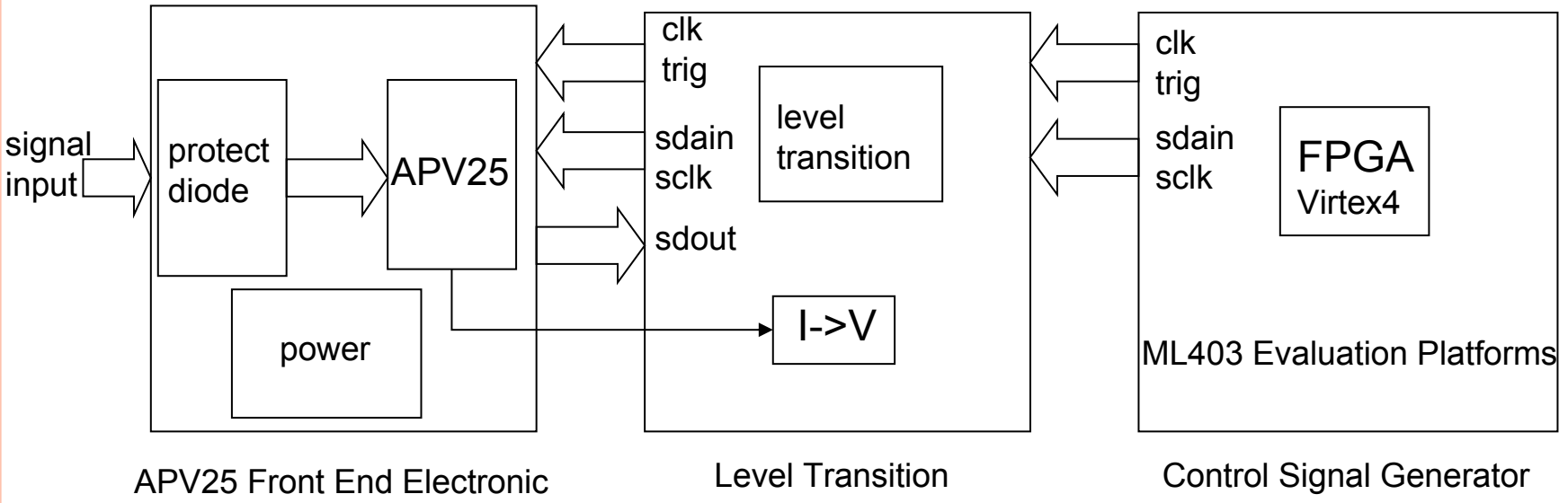
Contents

- Breif introduction to our lab
- Basic introduction to our test system
- Current test results
- Unsettled problems
- Further work

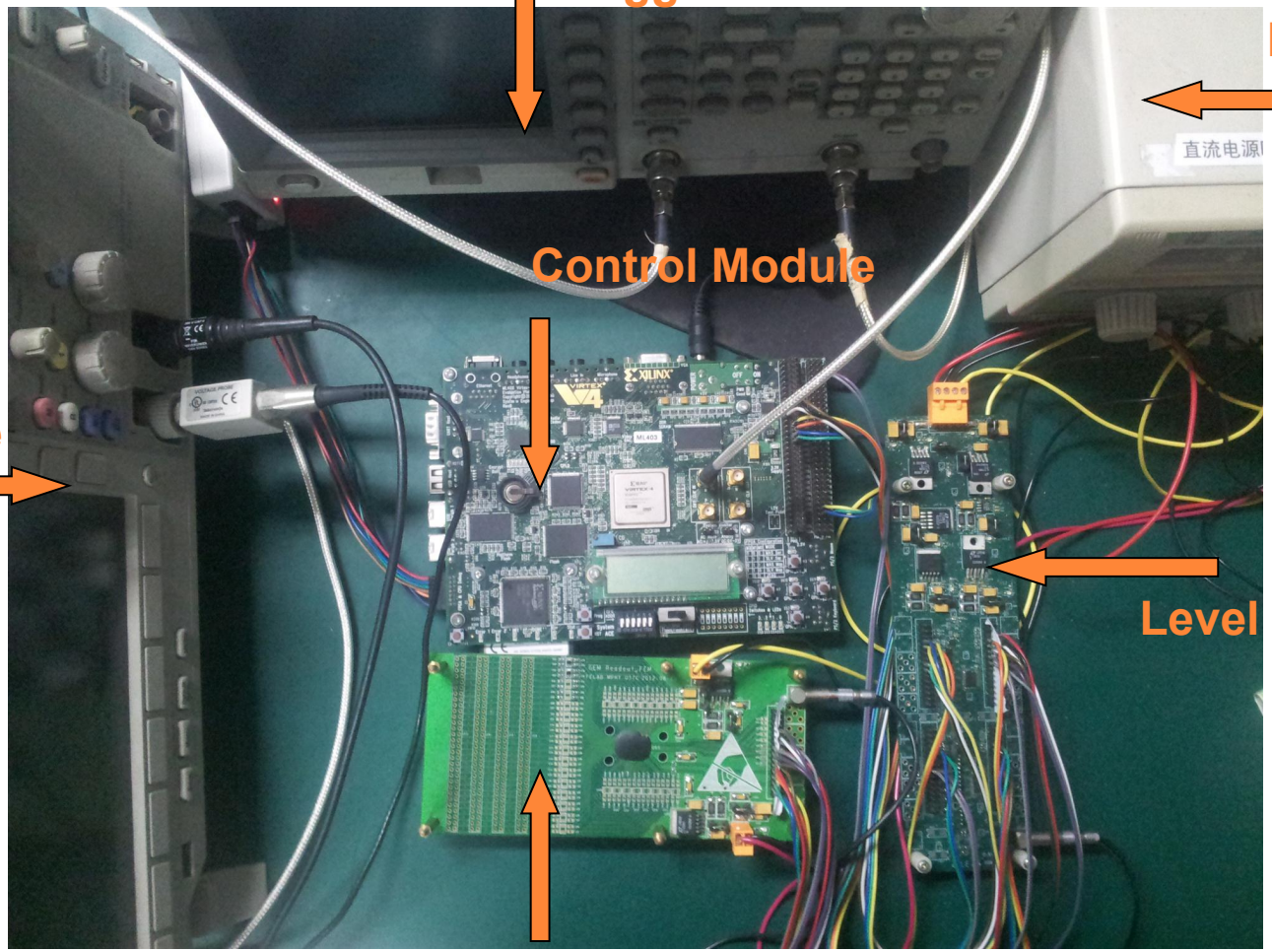
Lab

Our lab belongs to State Key Laboratory of Particle Detection and Electronics.
We target for world-class particle detection and electronics technology, and we have achieved great amount of research progresses. Now we have close cooperation with CERN CMS, ATLAS and BNL STAR groups. Also, our lab undertake many electronics for domestic large particle research project, like Daya Bay Experiment, BESIII upgrade, satellite detection of dark matter, etc.

System Block Diagram



System Photograph



APV25 Front End Electronic

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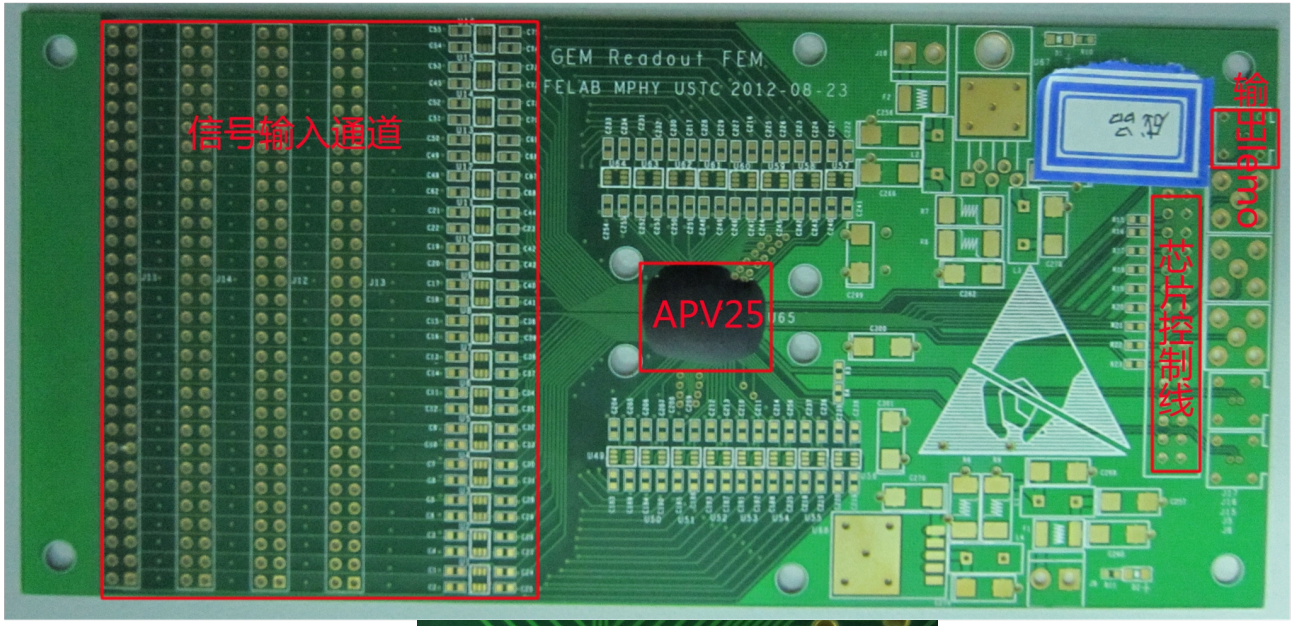
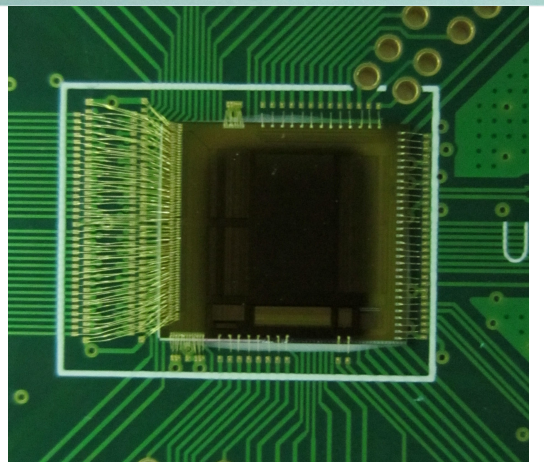


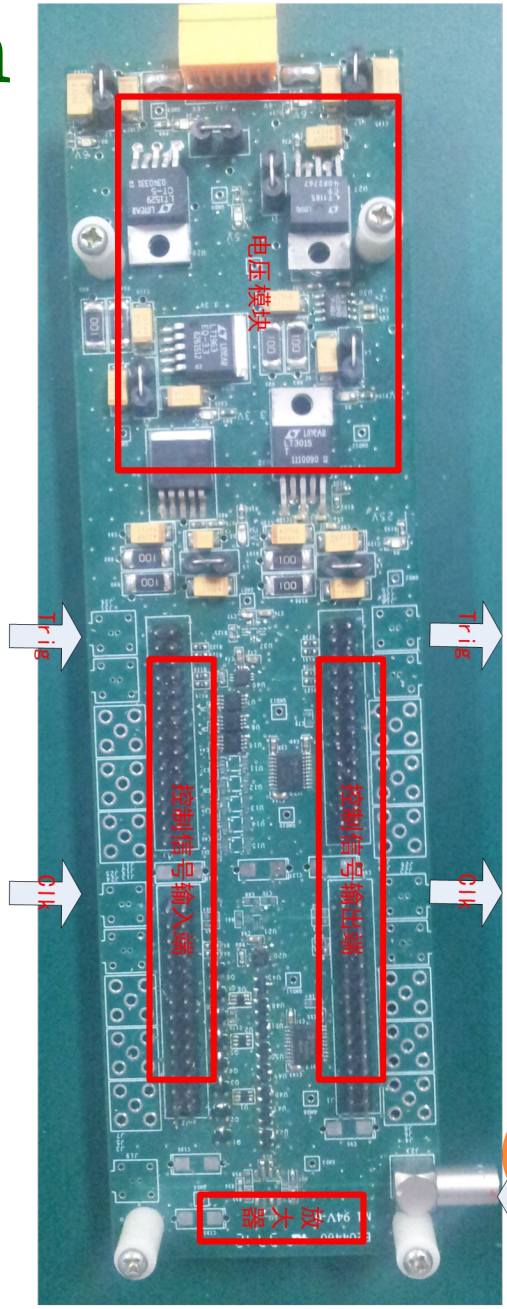


Level Transition

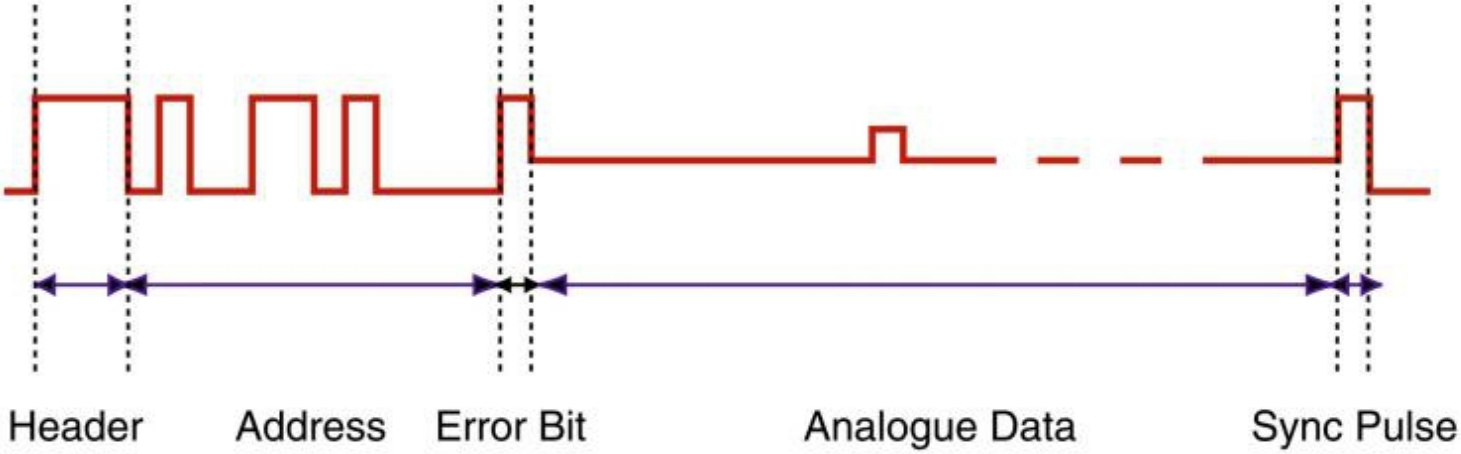
According to the APV25 User Mannel, the accepted logic level is +/-1.25V, while FPGA I/O logic level is generally 0/3.3V.

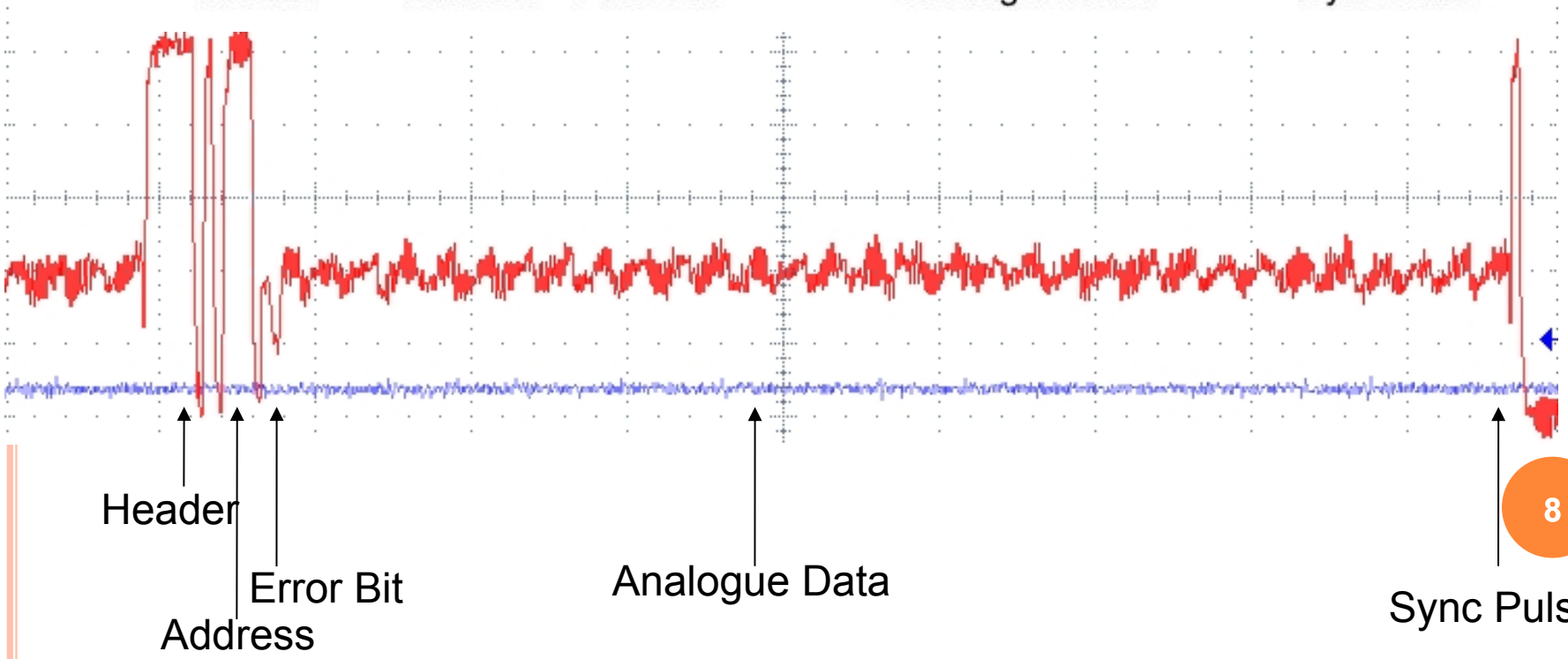
Also, the LVDS signal accepted by APV25 is -1.25V lower than normal.

However, in the following design, I hope to rise the whole voltage level of the Front End Electronic by 1.25V, thus to eliminate this level transition.

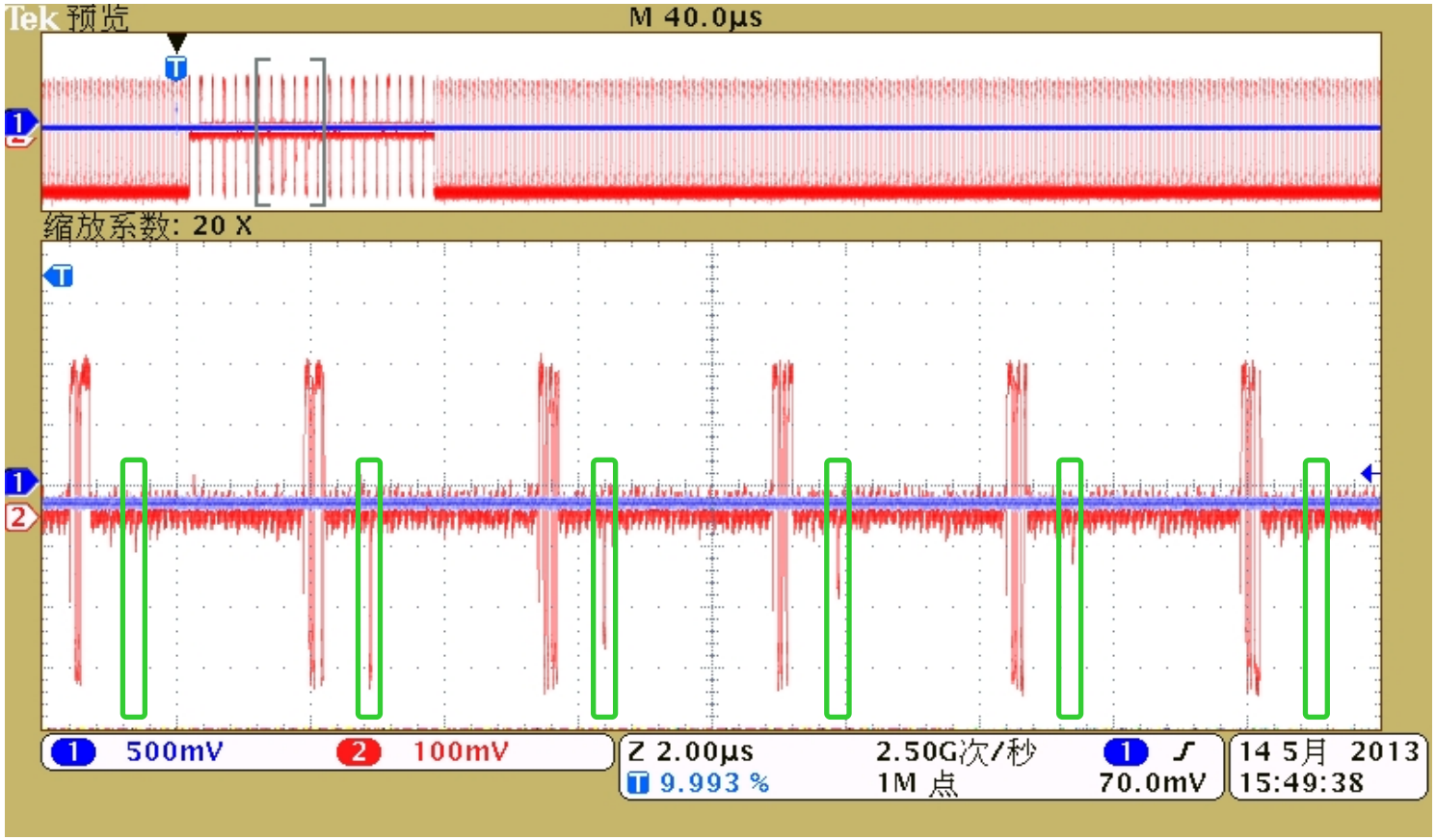


APV25 Output waveform



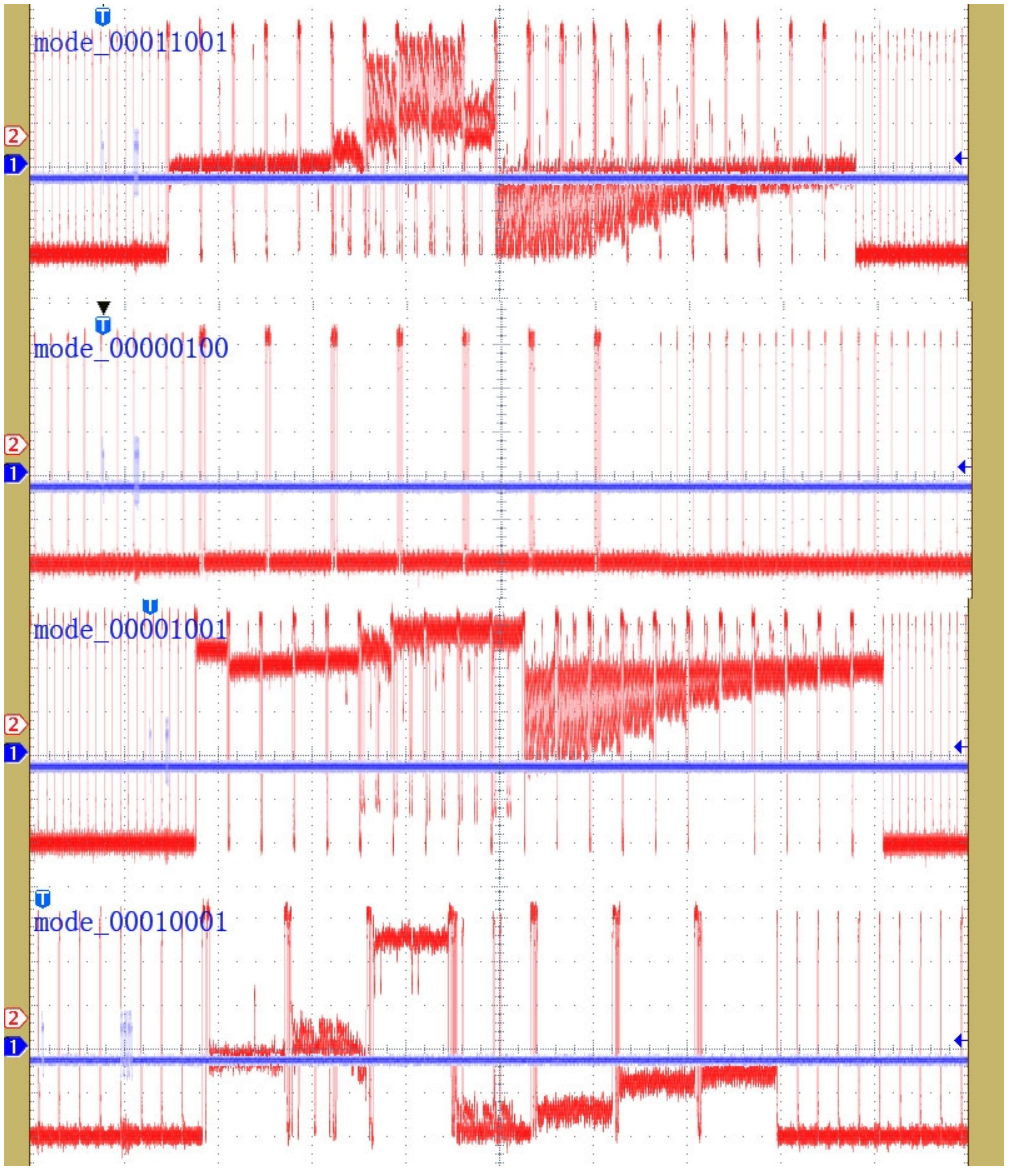


APV25 Output Waveform



Acquired by oscilloscope, in the mode of continuous triggers. Input signal from signal generator.

APV25 Calibration Mode

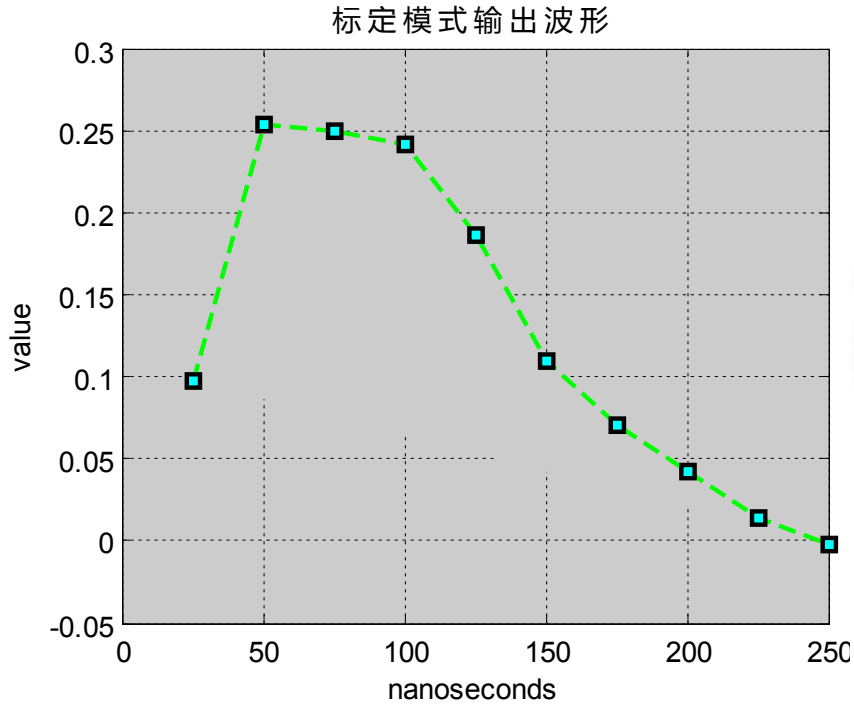


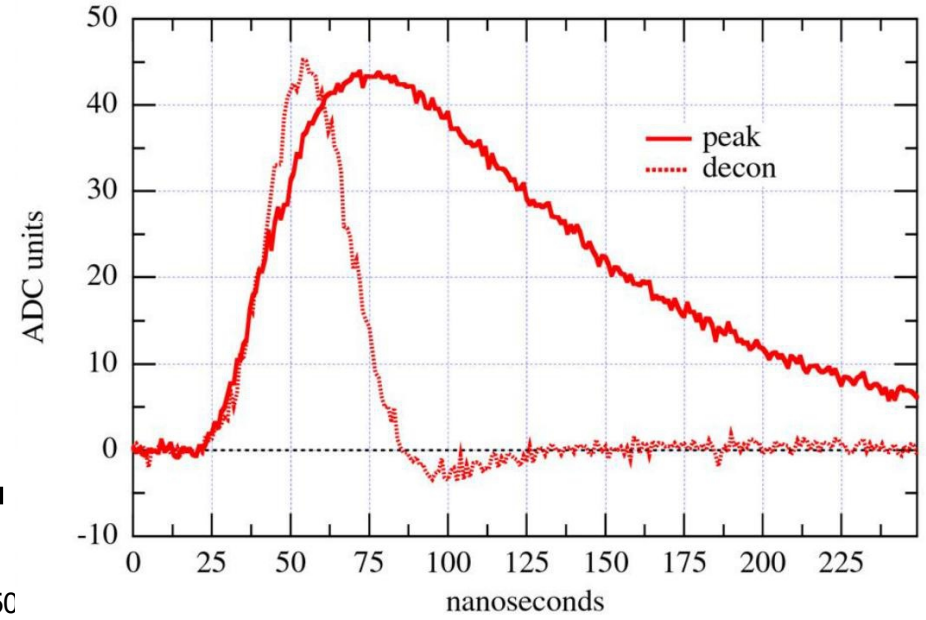
By changing the mode registor, I get different output waveform. But this result is very strange.

Also, changing calibration related registor values does not result in expected changes in test results.

Maybe the serrated waveform is the pedestal noise brought by calibration capacitance.

APV25 Calibration Mode





Consequentive sampling result of a channel

Further Work

- We decide to design a DAQ system for this APV board, or for other APV board we can access. In this way, we can control this APV chip more conveniently, and get the signal output more exactly.
- In this DAQ system, we hope to have a preamplifier, an ADC, a FPGA and related system. We hope to control 16 APVs and process their output simultaneously. Also, some algorithm can be implemented on this FPGA.

Thanks!