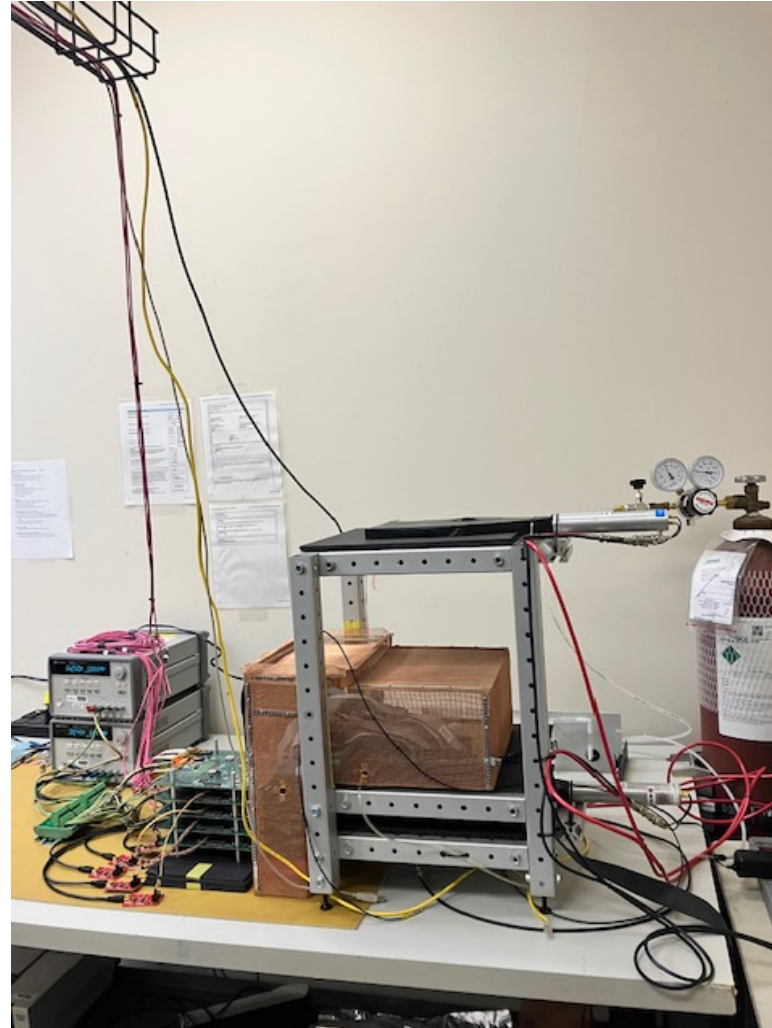


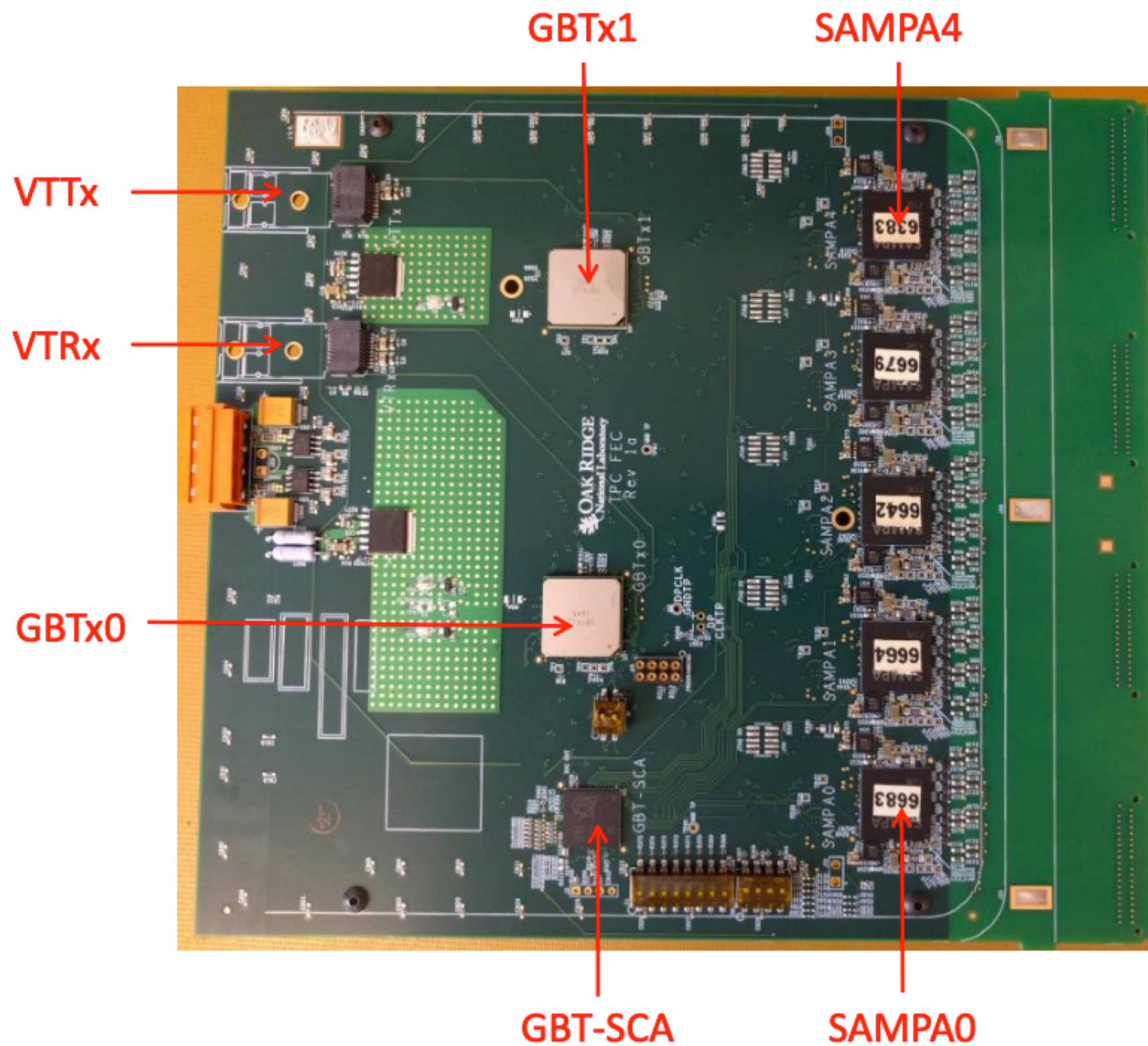
GEM Detector SRO

Data Stream Processing with ERSAP

GEM detector setup

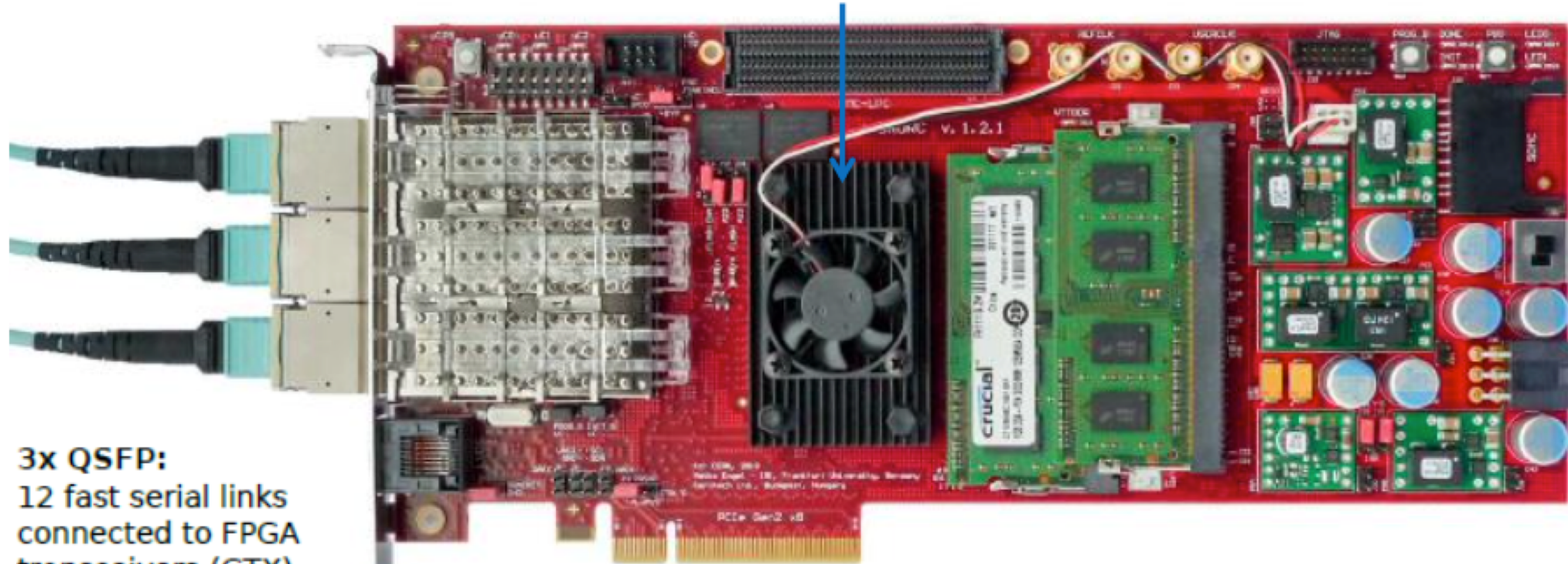


FEC – JLab version



C-RORC/T-RORC

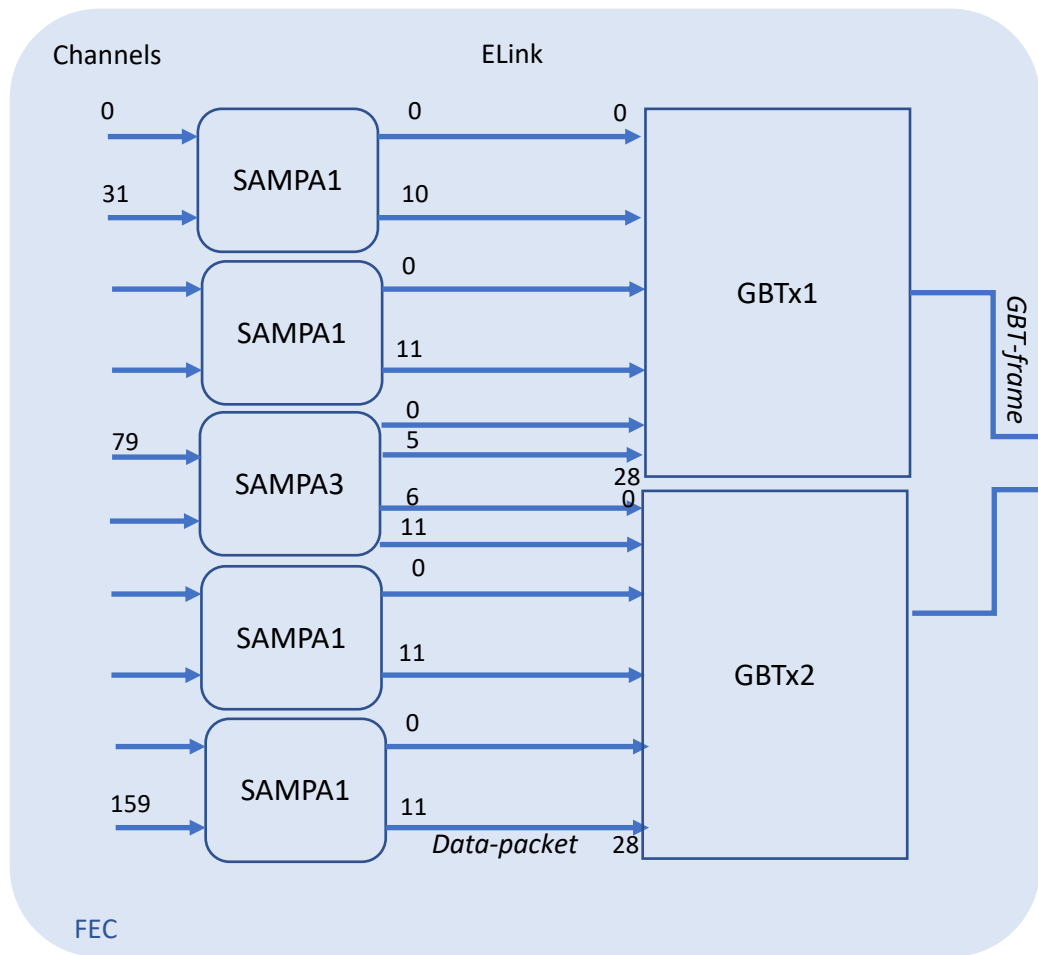
Xilinx Virtex-6 FPGA



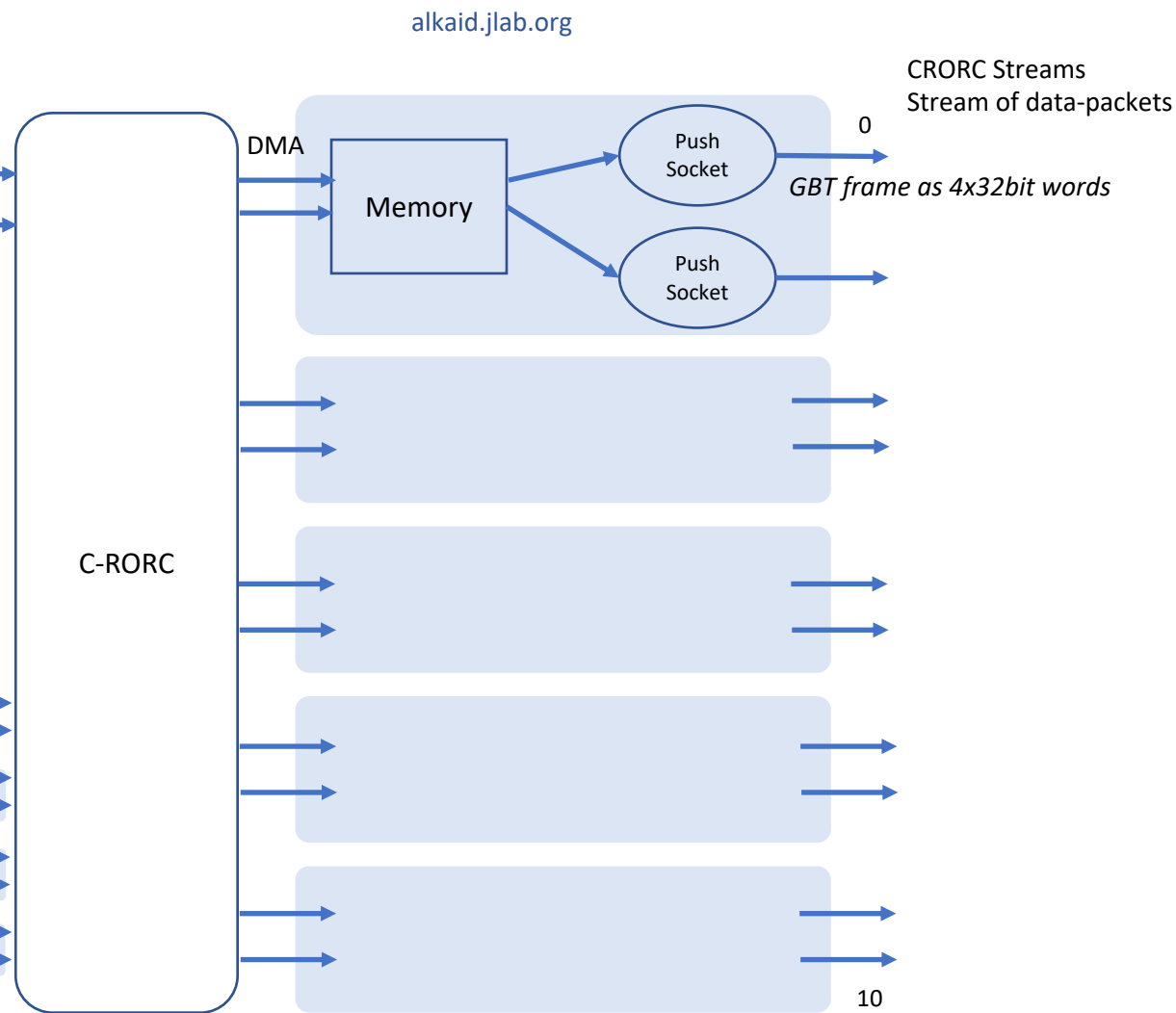
3x QSFP:
12 fast serial links
connected to FPGA
transceivers (GTX)
Up to 6.6 Gbps per
channel

PCIe Gen2, 8 Lanes
8x 5.0 Gbps, connected to
Xilinx PCIe Hard Block

(~ 30 Gb/s)



Front-End Components



Data-Packet

Packets every 50 μ sec at 20MHz sampling rate (i.e. packets every 1000 samples)

32bit word	Content
Packet Head-1	chip#, channel#, window-start-time
Packet Head-2	packet-type, words-in-packet, humming code
Data Head-1	number of ADC samples (e.g. N)
Data Head-2	time of the pulse in window
Data-1	10 bit value
Data-N	10 bit value

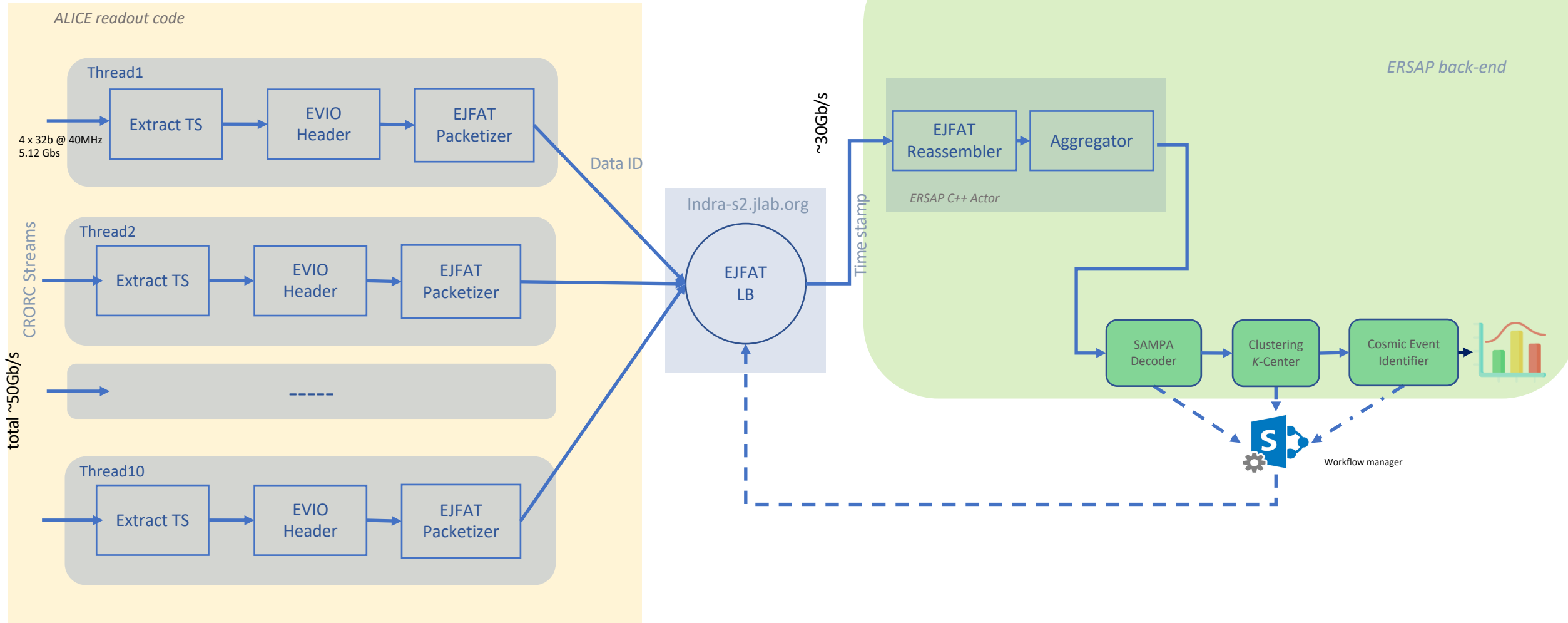
GBT Frame

- GBT wide frame format
- 120bits total, 112bits payload x 40MHz = 4.48 Gb/s
- Sent out every 25ns (40MHz)
- Data from a GBTx frame is pushed through the socket as a 4x32bit words

Prototype GEM detector SRO and processing

alkaid.jlab.org

ejfat-x-daq.jlab.org



Task	Start	End	Manpower	Comment
ALICE code modification to packetize and send data to EJFAT LB	09/15/22	10/3/2022	VG, CT	
EJFAT control plane			MG	
EJFAT reassembly			CT	
GBT streams aggregation and EVIO formatting			CT, VG	
SAMPA DSP decoder. ERSAP engine	09/20/22		VG	
GEM/SAMPA channel translation				
ML based clustering. ERSAP engine	10/3/22	10/24/22	VG	
Incorporating scintillating counters in the SRO			EJ	
Cosmic event identification. ERSAP engine			VG	
Real-time histogram. ERSAP engine	10/3/22	10/10/22	VG	

CLAS12 data-stream processing

